First-Phase Final Report (2013-2016)

# Self-Aware Computing for Cyber Physical Systems

Period: 1/Jan/2013 – 5/Dec/2016

**1. Personnel:**

- Mingoo Seok, Assistant Professor, Columbia University
- Peter Kinget, Professor, Columbia University
- Seongjong Kim, Graduate Student, Columbia University
- Teng Yang, Graduate Student, Columbia University

**2. Total Project Period:**

- 1/Jan/2013-31/Dec/16

**3. Project Goal:**

The goal of the project was to create a range of new techniques for making digital systems self-aware with temperature, device wearout, timing errors, and other high-level parameters, with which the systems can autonomously determine the operating settings for optimal performance, energy-efficiency, robustness, and reliability without the worst-case margin and over-design.

A key focus was to create techniques that are suitable for digital systems for resource-constrained cyber-physical systems applications. For the targeted applications, the critical requirements are low power dissipation, voltage scalability down to near/sub-threshold levels, and compact silicon footprint. Existing solutions often incur too much overhead in area, delay, and power dissipation, and thus wipe out a significant portion of the benefits of implementing self-awareness in digital systems. In this project, we have pursued the following research topics.

- **Analog sensors for on-chip temperature:** "One immediate research target in this proposal is to reduce the overhead of diverse analog sensors. We also want those sensors to operate at NTV regimes."
- **Analog sensor for device wearout:** "To design sensor cores (*temperature, process, and wearout*), we will exploit the novel design paradigm of 2T voltage references to replace pn-diode in the conventional temperature sensors and ring oscillators in the conventional wearout sensors."
- **Digital sensors for timing errors:** "We also plan to develop error sensors/detectors in digital circuits using error correction coding (ECC) and timing error detectors (TED)"
- **Models to extract high-level, difficult-to-measure parameters:** "we are interested in developing models to estimate the parameters that are not amenable to measurement with physical sensors."
- **Framework for optimal operating settings**: "We propose a comprehensive framework for self-aware digital design in CPSs. All the parameters, either instrumented or model-estimated, will be analyzed to determine the optimal operating policy online."
- **System demonstrations**: "we will demonstrate the key technologies via prototyping an ARM-compatible core and memory arrays. They are equipped with (i) a network of temperature, wearout, process sensors, (ii) error sensors/detectors (TED and ECC), and (iii) the associated energy and reliability models and framework for determining operating scenarios."

## 4. Research Results

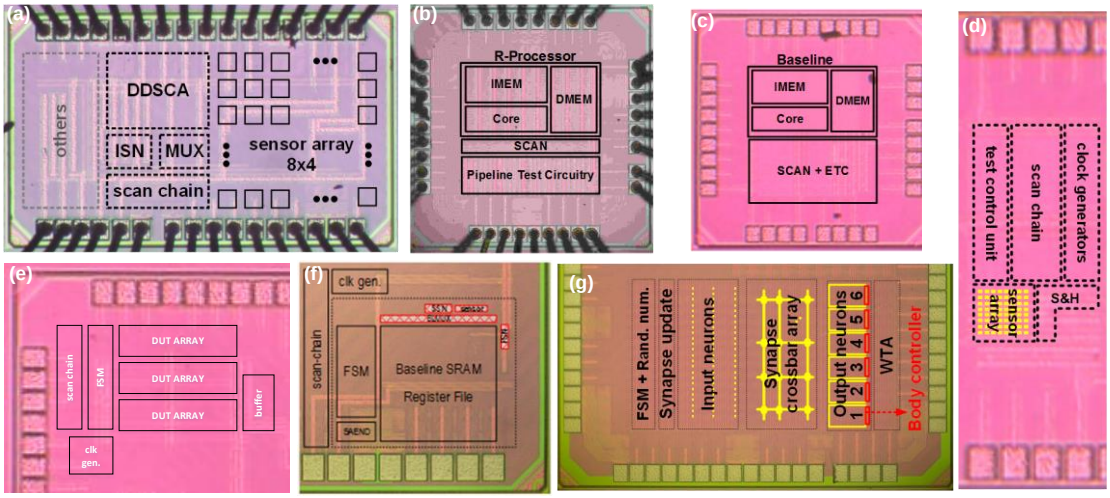


Fig. 1. Die photos of test chips prototyped in this project; (a) [Yang, ISSCC'14 & JSSC'15]; (b,c) [Kim, VLSI'14 & JSSC'15]; (d) [Kim, CICC'15]; (e) [Yang, ISSCC'15]; (f) [Yang, ESSCIRC'16]; (g) [Kim, VLSI'16];

Across the planned research items, we have made several critical advances in circuit designs and systems demonstrations. Several techniques enable *the first*, *the most compact*, and *the most voltage scalable* demonstrations. We have fabricated multiple test chips for this project over the last four years. We include some of the die photos of the test chips (Fig. 1). We summarize the current status and our evaluation in each research item in the table below.

| Planned items | Status |
|---|---|
| Analog sensors for on-chip temperature | • We have developed a thermal sensor with a sub-400μm$^2$ footprint, the worst-case error 7$^o$C after one temperature point calibration, and the minimum functional supply voltage of 0.6V. The results were published in [Yang et al., ISSCC'14] and [Yang et al., JSSC'15]<br>• We have developed a thermal sensor with a sub-30μm$^2$ footprint, the worst-case error 2.1$^o$C after one temperature point calibration, and the minimum functional supply voltage of 0.4V. The results were published in [Kim et al., CICC'15] |
| Analog sensors for device wearout | • We have developed the *first* technique to monitor device wearout in the digital pipelines *in-situ* and *in-field post-deployment*. The results were published in [Li et al.,, DAC'14].<br>• We have developed the *first* technique to monitor PMOS device wearout in the SRAM arrays *in-situ* and *in-field post-deployment*. The results were published in [Yang et al., ISSCC'15]<br>• We have developed more advanced technique to monitor both NMOS and PMOS device wearout in the SRAM arrays *in-situ* and *in-field* post deployment. The results were published in [Yang et al., ESSCIRC'16] |

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|---|---|
| Digital sensors for timing errors | • We have developed a sparse-insertion technique to reduce the overhead of error-detecting register insertion. The results were published in [Kim, et al., ISLPED'14] and currently in the third round review in [Jin et al., TVLSI'16]<br>• We have developed an error-detection and correction technique that is suitable for near/sub-threshold microprocessors. We prototyped a microprocessor with the technique. The results were published in [Kim, et al., VLSI'14] and [Kim et al., JSSC'15]<br>• We have developed an error-detection and -correction technique that is suitable for non Von Neumann architectures implemented in near/sub-threshold circuits. We prototyped a neural network accelerator for clustering tasks. The results were published in [Kim et al., VLSI'16]. |
| Models to extract high-level difficult-to-measure parameters | • We have developed a machine-learning model to estimate data retention voltage (DRV) and read access time ($T_{ACC}$) in SRAM based on the low-level threshold-voltage measurements from our proposed sensor circuits. The results were published in [Yang et al., ESSCIRC'16] |
| System demonstrations | • We prototyped a microprocessor with our first-generation EDAC technique [Kim et al., ISLPED'14, VLSI'15, JSSC'15]<br>• We prototyped a neural network processor with our second-generation EDAC technique [Kim et al., VLSI'16] |

We believe we achieve most of the goals we aimed in the beginning of the project. We create techniques to make digital systems to be self-aware with various parameters to make optimal decisions to push the performance, energy-efficiency, reliability, and robustness under varying conditions.

## 5. References


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