uWatt Computing: Application-Driven Circuits and Architectures for Wireless Sensor Devices

David Brooks, Matt Welsh, and Gu-Yeon Wei
School of Engineering and Applied Sciences
Harvard University

Final Project Report

This will serve as the final report for Catalyst Foundation project conducted at Harvard University for the time period of January – December 2006.

We have four major contributions to discuss.

- We completed the design (RTL, circuit design, and chip layout) of the first version of the sensor node compute chip. This chip implements many of the key architectural concepts from our ISCA 2005 paper and provides an initial proof-of-concept of the approach. The chip taped out in February 2006 and returned from fabrication late in the Spring. We performed extensive testing over the summer of 2006 and were able to achieve limited functionality. The design received 1st prize in the SRC SoC design contest and provided a valuable learning experience for our research group. The RTL and circuit design will be levered for future implementations and for additional simulation-based research activities. We plan a second chip tape-out in March of 2007 which we hope will enable full functionality of our sensor node.

- We performed a detailed simulation analysis of the optimal choice of process technology for low-throughput wireless sensor applications. We study these issues in the context of our sensor node architecture that provides explicit support for fine-grain leakage-control techniques such as Vdd-gating and adaptive body bias. Our results show that leakage power will dominate the selection of process technology, and architectures that support advanced leakage control techniques at the circuit level will be essential. We find that without advanced low-power architectures future nano-scale process technologies will not be suited for sensor network applications. This work has been published in the IEEE/ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), October 2006.

- We performed a study analyzing the impact of customization for embedded architectures in the energy-constrained domains of sensor and multimedia processing. We present an approach to analyze the runtime profiles of applications and combine this information with a model for our architectural design space providing a robust customization engine built upon a fully automated method for determining an efficient architecture (together with appropriate application transformations). The approach shows that significant energy savings can be achieved with architectural customization and suggests that heterogeneous CMPs can be a cost-effective approach to capitalize on this

potential. This work resulted in a second publication in the IEEE/ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), October 2006.

- The project provided opportunities for research and practical hands-on design experience for two graduate students (Mark Hempstead and Xiaoyao Liang) and two undergraduates (Patrick Mauro and Lukasz Strozek). Both Patrick and Lukasz worked directly with our research team in designing the first version of our sensor node compute element and conducting research activities.

Publications:

Mark Hempstead, Gu-Yeon Wei, and David Brooks, "Architecture and Circuit Techniques for Low-Throughput, Energy-Constrained Systems Across Technology Generations," IEEE/ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), October 2006.

Lukasz Strozek and David Brooks, "Determining Efficient Custom Embedded Architectures Based on Runtime Profiles of Applications," IEEE/ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), October 2006.

Mark Hempstead, Xiaoyao Liang, GuYeon Wei, David Brooks. "An Event Driven SoC for Sensor Network Applications: Silicon Evaluation," SRC Student Symposium 2006, Invited Paper: SoC design contest Final Phase, 1st Prize. Cary, NC, October 2006.