

Final Report for Supplemental Award
Wireless Optical Sensors for High Resolution Imaging of Biological Structures
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Abstract

In order to fully utilize the capabilities of Si integration for Near Infrared Spectroscopy, a 4-channel optical sensor front-end and signal processing circuits have been integrated on a 180nm, 2.25mm² CMOS chip. The estimation of optical parameters by measuring the amplitude and phase changes in the modulated laser diode has been implemented using an off-chip time-to-digital converter on an FPGA. The complete system has been characterized electrically and an optical test-bench using a homogeneous tissue phantom has been used to evaluate the performance of the chip. This report summarizes the design and enlists future work.

I. Introduction

The characterization of the structural and physiological properties of tissue using frequency domain near infrared spectroscopy (fdNIRS) requires measurements taken at linearly spaced spatial locations. Near Infrared spectroscopy is a non-invasive technique used to measure oxy and de-oxy hemoglobin concentrations of tissue by using the scattering and absorption coefficients at multiple NIR wavelengths[1]. An optical sensor array has been integrated on a 2.25mm², 180nm CMOS chip. The individually addressable sensor array enables concurrent measurements as required in multi-distance fdNIRS. The changes in amplitude and phase at multiple distances from the source are measured to specifically calculate the absorption and scattering coefficients of the tissue. Each sensor in the 4-channel array consists of a 22THzΩ transimpedance amplifier to detect light modulated at 110MHz followed by a heterodyned architecture along with amplitude and phase detection circuitry based on pulse width modulation and zero-crossing detection. The sensor draws less than 40mA of current from a 1.8V power supply. An FPGA based counter is used to resolve time delays with a 20ns resolution corresponding to a 0.288° phase resolution. The 0 – 360° phase detector has a maximum measured linearity error of < 2.5%. The amplitude detector has a maximum measured linearity error of < 6.5% for modulation depths between 20% and 80%. Sensor performance is measured using a homogeneous tissue phantom to observe the change in phase and amplitude with maximum linearity error of < 8%.

II. Circuit Architecture

Fig. 1 shows the architecture for the 4-channel optical sensor array. Hamamatsu S9251-15, APDs are used as external photodetectors. These photodetectors have a high responsivity of 15A/W in the NIR region, a parasitic capacitance of 3.6pF along with low dark current making them suitable for low light and high frequency detection. A 22THzΩ transimpedance amplifier is designed using a 3-stage voltage amplifier to provide low noise detection and conversion of the 110.04MHz current received from the off-chip APD to a voltage. The 110.04MHz signal is down-converted using a mixer to a 40kHz signal [2]. In this technique the useful information is the AC amplitude of the signal and the phase delay. Hence, a power hungry ADC is avoided by converting the AC amplitude and the phase delays into pulse modulated waveforms and delayed square waves as

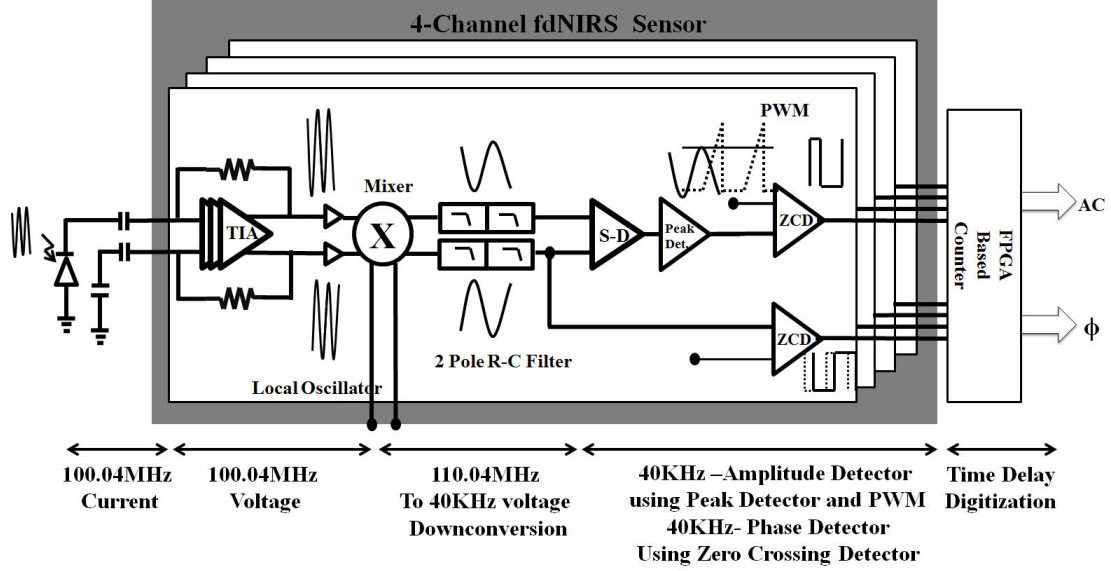


Figure 1: Architecture of the heterodyned optical sensor array and signal processing circuits.

shown in fig. 1. In addition to the simplicity of this technique, it enables off-chip quantization and calibration using a counter based time-to-digital converters (TDCs) on an FPGA [3],[4].

In a homogeneous medium the AC amplitude reduces exponentially with distance while the phase difference increases linearly. The amplitude ($AC(r)$) and phase ($\phi(r)$) data recorded at multiple source-detector separation distances (r) are used to plot the linear functions $\ln(AC(r) * r^2)$ vs r and $\phi(r)$ vs r . The slopes of these lines, S_{AC} and S_{ϕ} , are used to calculate μ_a and μ'_s using equations 1 and 2.

$$\mu_a = \frac{\omega}{2v} \left(\frac{S_{\phi}}{S_{AC}} - \frac{S_{AC}}{S_{\phi}} \right) \quad (1)$$

$$\mu'_s = \frac{S_{AC}^2 - S_{\phi}^2}{3\mu_a} \quad (2)$$

A heterodyned architecture is used to reduce the signal processing circuit complexity. The 110.04MHz signal is down-converted to a 40kHz signal. For phase detection, the 40kHz sine wave is converted to a square wave using a zero-crossing based comparator[3]. The phase change delay is proportional to the time delay between the rising edges of the square waves. For amplitude detection, a peak detector generates a DC voltage corresponding to the peak of the down-converted signal. This DC signal is converted to a pulse width modulated waveform using a comparator and a ramp signal as shown in fig. 1. Each of the 8 waveforms can be quantized using off-chip counter based TDCs. The heterodyned architecture also provides a platform to detect multiple wavelengths modulated at slightly different frequencies. This is critical for the detection of multiple chromophores that are present in the tissue.

The choice of modulation frequency affects the signal to noise ratio (SNR) of the measurement. Higher phase SNR requires a higher modulation frequency while a slower modulation frequency

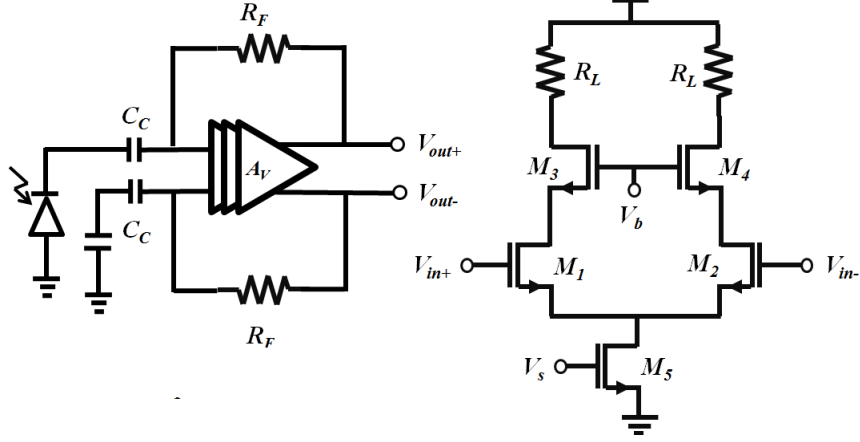


Figure 2: Differential transimpedance amplifier and single stage of the core voltage amplifier.

simplifies detector electronics and reduces circuit noise, resulting in a larger amplitude SNR. Hence as a trade-off a frequency of $110MHz$ is chosen by commercial instruments [1, 5, 6, 7, 8].

III. Design and Simulation

Transimpedance Amplifier Design

A resistive feedback TIA with $100k\Omega$ transimpedance and $220MHz$ bandwidth is designed as shown in Fig. 2. The TIA, adapted from [5], consists of a fully differential three-stage core voltage amplifier with $60dB$ gain. Each stage (Fig. 2) in the TIA is a differential amplifier with cascode transistors M_3 and M_4 . A large input transistor with a large gate-to-source capacitance of $C_{gs} = 3.6pF$ is designed to match the parasitic capacitance of the APD to ensure optimized noise performance. The following stages have an input transistor with only $50fF$ capacitance. With the overall input capacitance ($C_{in} = C_{gs} + C_{pd} = 7.2pF$) and a feedback resistor of $100k\Omega$, the required gain for the voltage amplifier (A_v) using Equation 3 is $60dB$ to obtain the required bandwidth of $220MHz$ to ensure $3dB$ flatness at the required $110MHz$ frequency for the overall TIA.

$$f_{TIA} = \frac{A_v}{2\pi R_F C_{in}} \quad (3)$$

In order to ensure sufficient phase margin of 60° , the bandwidth of the core amplifier is designed to be 4 times the TIA bandwidth. Hence each stage of the core amplifier is designed to have a bandwidth of $1.9GHz$ by using the appropriately sized cascoded transistors to obtain an overall bandwidth of $880MHz$. The drain-to-source capacitance of the cascoded transistors is smaller than that of the input transistors hence pushing the output pole as far as possible to achieve the high bandwidth. The obtained input referred noise is $181nA_{rms}$.

Down-Conversion Mixer and Filter

A Gilbert Cell Mixer without the tail current source is used to down-convert the $110.04MHz$ signal to a $40kHz$ signal using an external oscillator. The mixer has a simulated linearity of $2.6dbm$

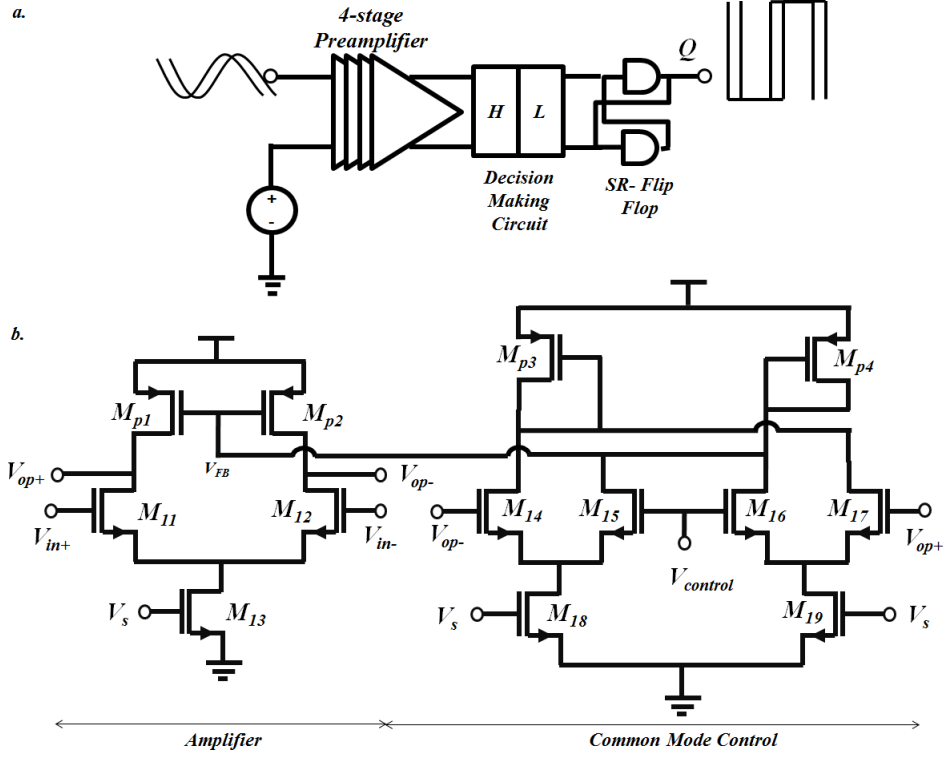


Figure 3: a) Block diagram of the high-speed comparator, and b) Preamplifier circuit using a common-mode feedback based OTA.

and consumes $2mA$ current per channel. The mixer generates the $40kHz$ signal as well as a high frequency as a result of the non linear mixing which is filtered out using a simple two stage R-C filter. A common drain amplifier stage isolates the TIA and mixer while also ensuring appropriate biasing of the mixer.

Phase and Amplitude Detection

The phase difference between each sensor is measured by quantizing the time delay between each channel. The time difference is converted to phase by using equation 4.

$$\phi = \frac{t_d * 360}{T} \quad (4)$$

where, t_d is the measured time difference, T is the period of the signal and ϕ is the phase difference. To facilitate the measurement, the $40kHz$ sine wave is converted into a square wave using a zero crossing detector (ZCD). The ZCD is designed using a high-speed comparator as shown in Fig. 3. The sine wave is compared with a dc signal corresponding to the dc level of the sine wave. The comparator is designed using four cascaded OTAs as preamplifiers followed by a positive feedback decision making circuit and an SR-Flip Flop. Four preamplifiers, as shown in Fig 3, based on the common mode feedback based OTA adapted from [9] are used before the decision making circuit to ensure sufficient gain.

The dc signal $V_{control}$ is used as the zero-crossing DC voltage as well as the common-mode reference of the preamplifiers. This ensures accurate ZCD without common-mode errors. The

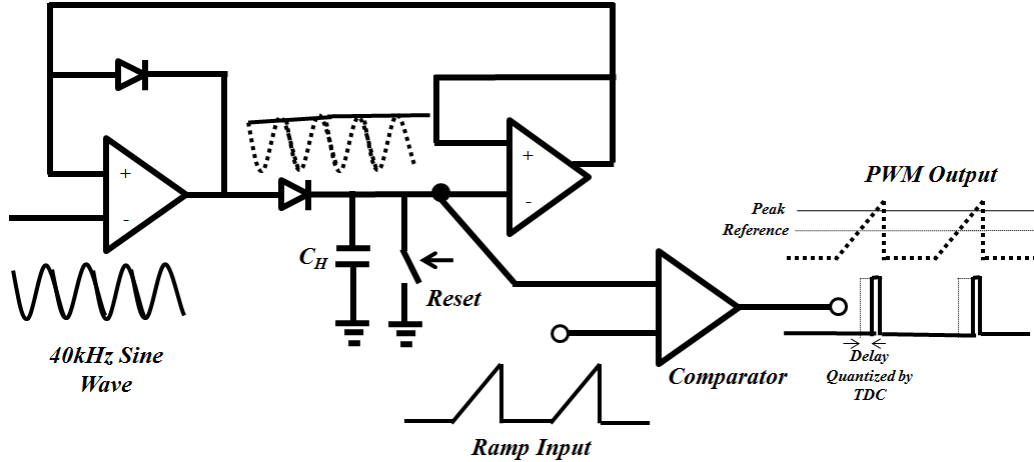


Figure 4: Block diagram of the amplitude detector circuit.

decision making circuit is designed using a differential positive feedback regenerative amplifier followed by a standard NAND gate based S-R Flip Flop.

The AC amplitude is detected by using an OTA based peak detector shown in Fig. 4. The dc output of the peak detector corresponding to the peak amplitude of the AC signal is then converted into a pulse width modulated waveform by using a comparator as in Fig. 3 where the input dc is compared with a $10kHz$ ramp signal. The width of the pulse can be quantized similar to the phase delays using an external counter.

IV. Test and Measurement

Electrical Characterisation

An Electro-optical PCB shown in fig.5, is designed to test the IC. The photodetectors are placed 1cm away from each other while the size of the PCB is small enough to ensure the distance between the first detector and the laser can be set to 2cm. This is required to ensure that light detected is the diffused light from the tissue phantom rather than just stray light from the source.

The CMOS chip draws $38mA$ of current from a $1.8V$ power supply. An electrical testbench is used to observe the down-conversion of the signal and measure the linearity of the phase delay measurement by modeling the APD by a current source in parallel with a $3.6pF$ capacitor. The constant offset delays between each channel are measured and used for calibration. A $50MHz$ counter based FPGA is used to quantize the time delay. This technique is used to measure phase differences of $0 - 360^\circ$ corresponding to time delays upto $25\mu s$ for a $40kHz$ signal. The $50MHz$ clock provides a $20ns$ resolution while the counter counts from 0-1250.

The linearity error of the optical sensor channel is $<2.5\%$. For calibration, this is measured by using two sensor channels on the chip which reduces errors due to mismatches as well as synchronization errors. The high frequency sine wave input to one channel is constant while the phase of the the other channel is varied from $0 - 360^\circ$. The down-converted square wave phase output of the chip is applied to the FPGA based counter where the rising edge of the constant channel starts the

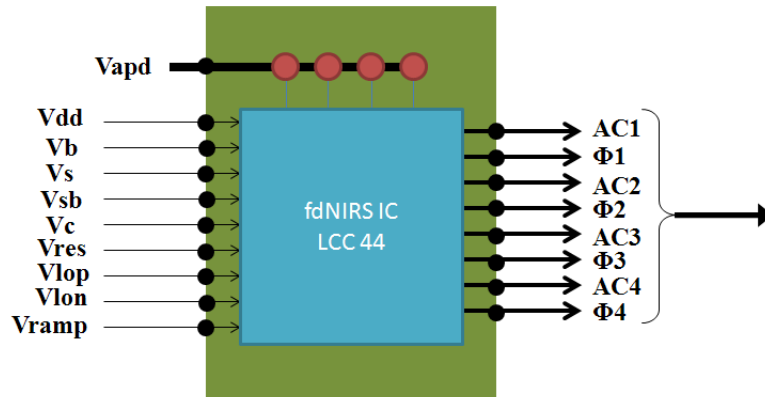
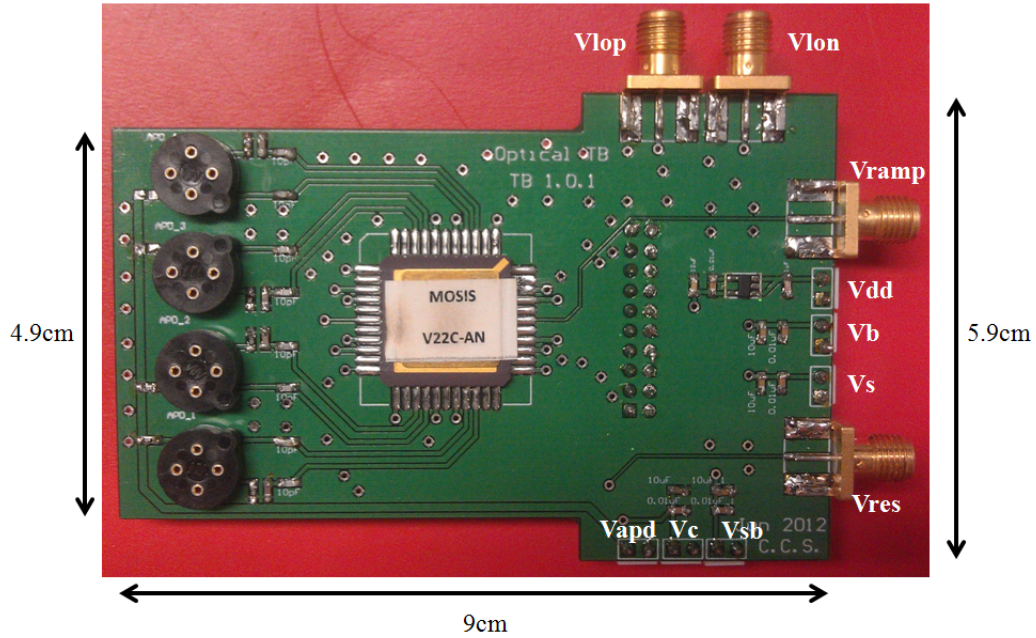


Figure 5: Electro-optic PCB for characterization of the fdNIRS chip

counter and the rising edge of the delayed channel stops the counter. The measurement technique will be explained further below. The graph of observed counts vs phase difference is plotted in Fig.6 along with the linear fit and the % Linearity error.

Tissue based Optical Characterisation

An experiment using a tissue phantom as shown in Fig. 1, is set up to measure the phase changes observed by one sensor as the distance between the source and detectors is varied. Using one channel of the CMOS based design, the sensor-detector distance is increased in steps of 0.125cm from 2cm. Fig. 7 shows the measurement setup and Fig. 8 shows the operation of the counter based time quantizer. Similar to the previous experiments, another channel is used as a reference to minimize errors due to synchronization. The measured phase count versus distance is plotted in Fig.9. As expected for a homogeneous medium, the phase increases linearly with the distance.

Table 1: IO Key for characterization PCB

Pin Name	Signal	Function
Vdd	6V Supply to 1.8V	Main Supply LDO
Vb	1.6V	Miller Transistor Bias
Vs	0.65V	Tail Current Bias for TIA
Vsb	0.65V	Tail Current Bias for Mixer, Comparator
Vc	1V	Comparator Common Mode Bias
Vres	1Hz, 0-1.8V	Amplitude Detector Reset
Vlop and Vlon	110MHz	Mixer Local Oscillator
Vramp	10kHz	Ramp for PWM Generator
Vapd	180V, 100uA	APD Bias
AC1-4	0-1.8V PWM	AC Output
Φ1-4	0-1.8V ZCD	Phase Output

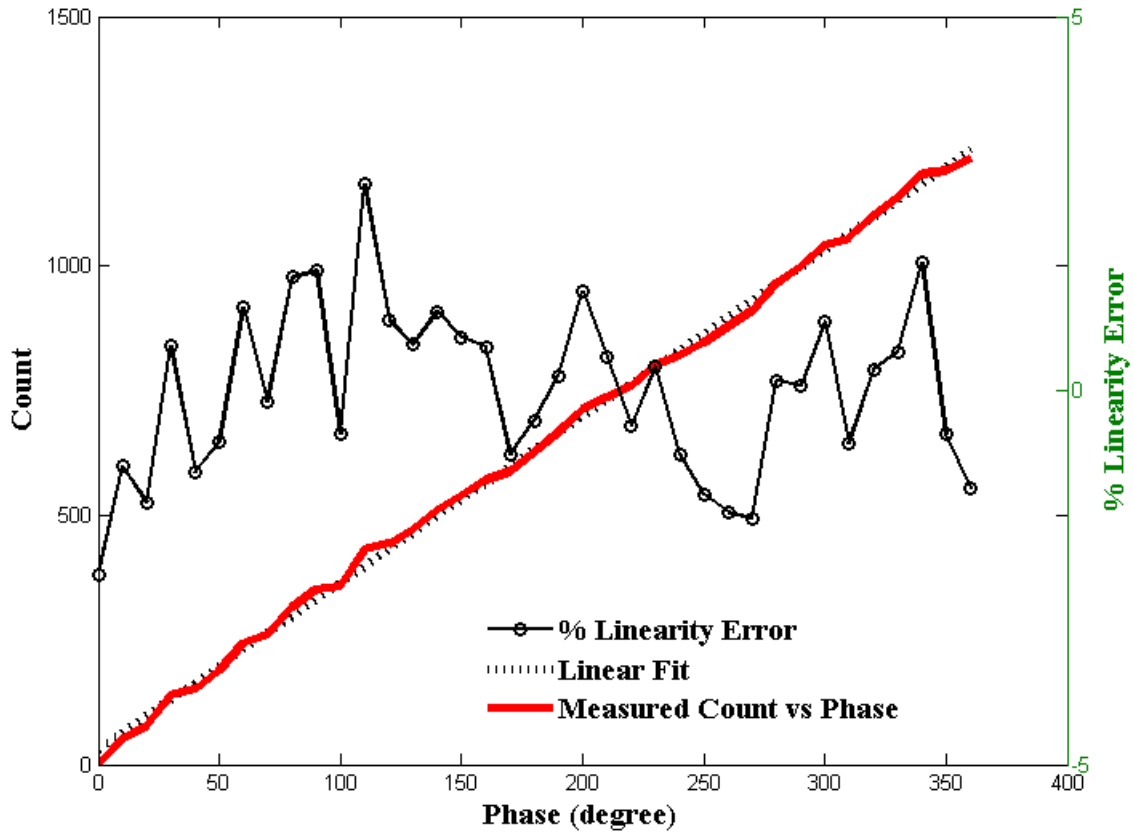


Figure 6: Plot of the measured count and the % Linearity error vs. phase difference.

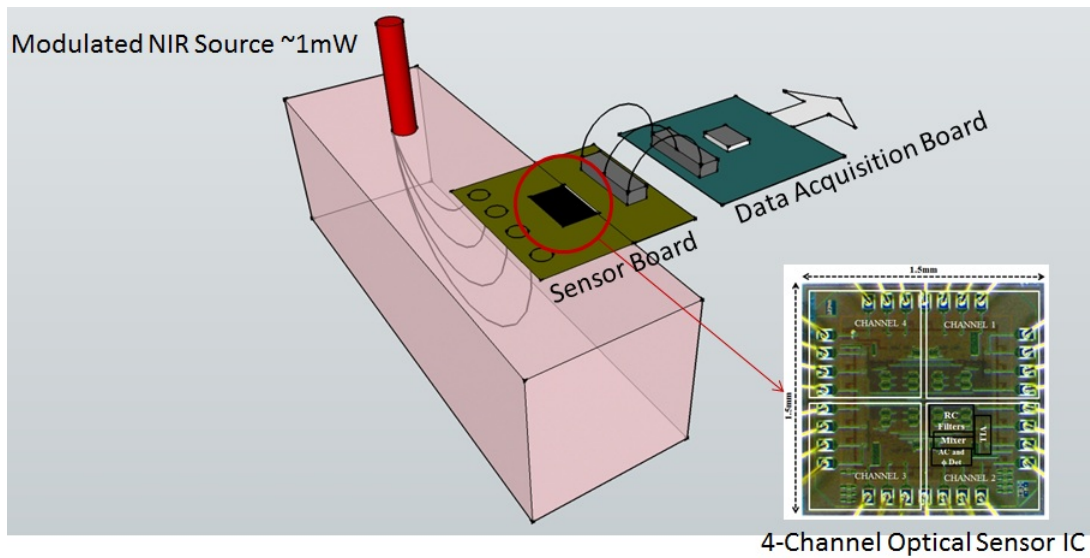


Figure 7: Setup for measurement and characterization of the fdNIRS chip using a tissue phantom and an FPGA based counter

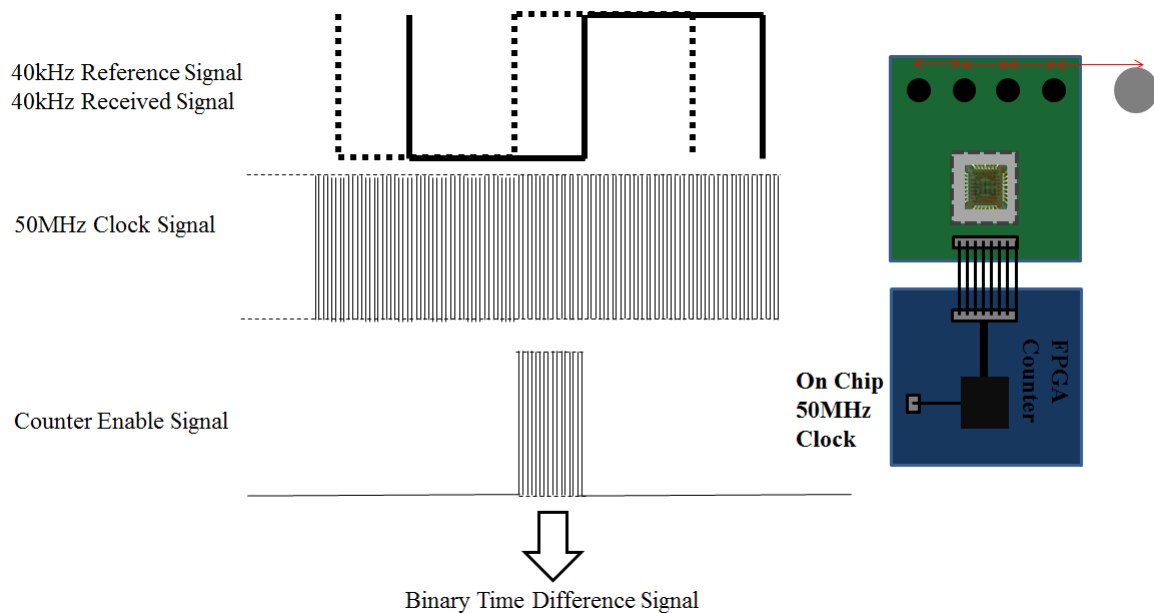


Figure 8: FPGA Counter based time delay measurement to quantize phase delay as well as PWM amplitude waveforms

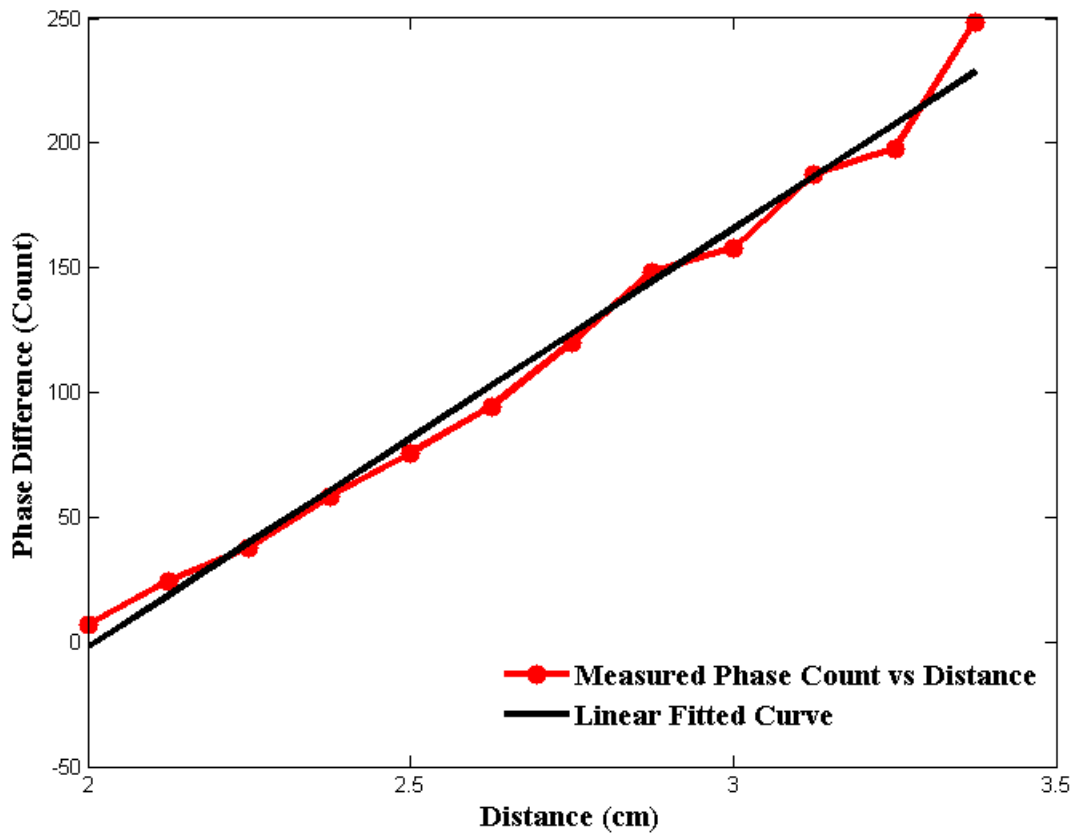


Figure 9: Plot of Phase(ϕ) vs Source-detector separation distance (r) for a homogeneous tissue phantom

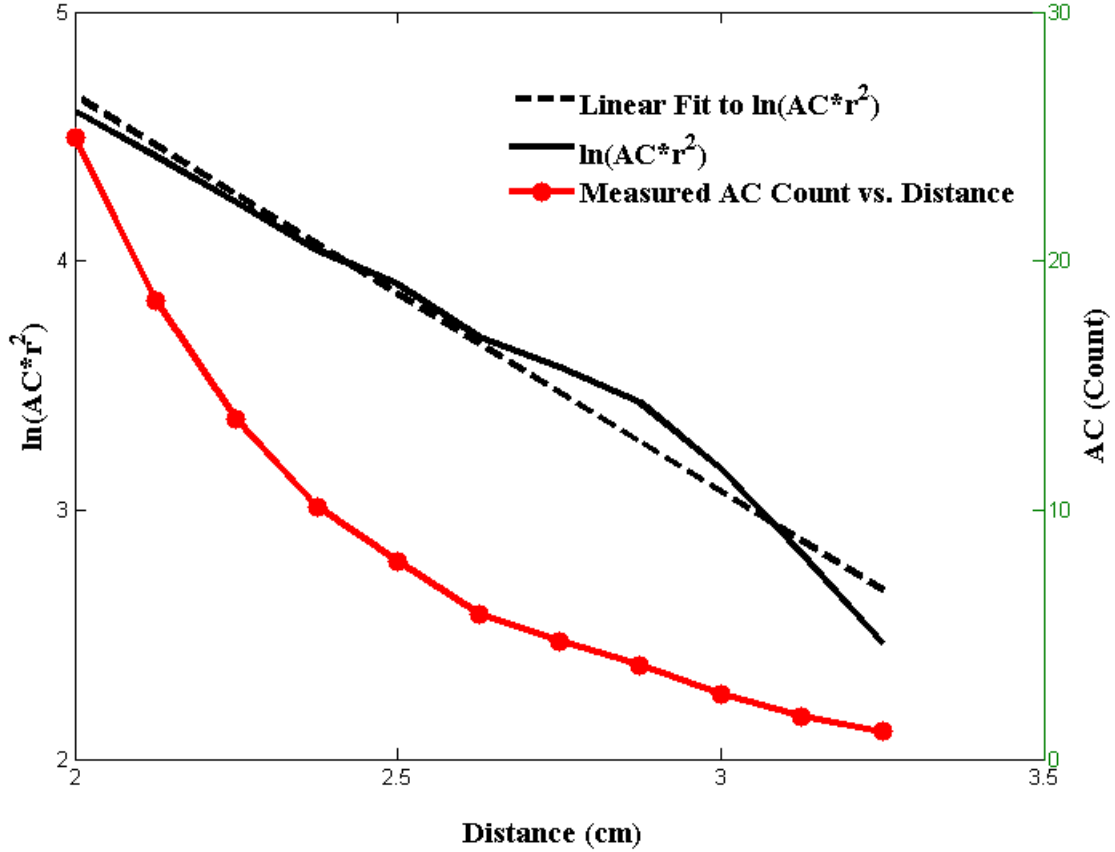


Figure 10: Plot of AC Amplitude and $\ln(AC(r) * r^2)$ vs Source-detector separation distance (r) for a homogeneous tissue phantom.

The change in amplitude with increase in source detector separation is plotted in fig. 10. An optical test-bench is used to measure the amplitude response of the tissue phantom. Two channels are used for this measurement. A $110.04MHz$ modulated $690nm$ laser diode is incident onto the tissue phantom. The change in the pulse width with reference to a constant second channel is measured using the FPGA. The distance between the source and detector is varied in steps of $0.125cm$.

As expected for a homogeneous tissue phantom the AC amplitude reduces exponentially as shown in fig. 10. The exponential nature of the AC curve is verified by plotting $\ln(AC(r) * r^2)$ vs r and observing the linear nature of this curve.

V. Future Work

The heterodyned approach used in this chip increases the accuracy of the measurement. But, to achieve this accuracy it is essential to ensure that the local oscillator used for the down-conversion is a pure tone with low jitter. Since the LO is supplied externally, the interconnect wires introduce delays and significant jitter. Hence, oscillators will be integrated on-chip with low phase noise.

To further our goal of increased spatial resolution for NIRS, we will research techniques to use on-chip photodetectors and the electronics required therein.

The data acquisition is a key feature of this research. We are currently using an FPGA based

time-to-digital converter(TDC) to quantize the phase and amplitude instead of using a high power ADC. While this technique provides flexibility in measurement and data recording, the TDC will be integrated on chip to enable wireless digital communication between the sensor and a data logger.

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