Research on Generalized Radix Design of Low-Power High-Performance Pipelined & Cyclic ADCs
Final Report

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Abstract

The power efficiency of pipelined and cyclic ADCs can be improved significantly by judicious choice of the interstage gain. Previous investigations by the authors have shown the possibility of using a novel technique known as the generalized radix design approach to attain the goal of optimal power-speed tradeoffs in this class of ADCs. In order to test the proposed methodology, a prototype pipelined ADC utilizing the aforementioned technique has been designed and will be fabricated and tested in the coming months. This design utilizes several circuit techniques to achieve the high level of performance and power efficiency. This particular ADC is expected to find widespread usage in several fields including medical imaging, biomedical applications, video and communication.

1. Introduction

Pipelined ADCs find widespread usage in several applications ranging from consumer electronics to sophisticated medical imaging applications. Cyclic ADCs are the dual of pipelined ADCs and find usage in low-power, moderate-speed applications. Such applications include blood-sugar detection meters, instrumentation etc. Power efficiency is of paramount importance in all these applications, and several techniques have evolved in this field to attain high levels of efficiency at circuit and system level. However, certain gaps in the system level design prevent the attainment of the highest levels of power efficiency in these ADCs.

Investigations by the authors have resulted in a better understanding of these issues, and development of a generic system-level design approach called the *generalized-radix design technique*. This involves using the optimal interstage gain to maximize power efficiency of these devices. The details of this approach can be found in [1],[2]. This technique departs from the conventional schemes that use interstage gains of the form 2^N, thereby leaving gaps in the design space, where the optimal realization may lie. The proposed scheme allows realization of any integer-level interstage gain with a minimal design overhead, thereby affording low-cost realization of highly efficient ADCs. If required, additional enhancements such as digital calibration may be added to improve the sensitivity of these devices. It is expected that power efficiency of a pipelined ADC can be boosted up by 30% - 50% through the use of the proposed technique. For high-performance converters, this represents a significant improvement.

2. Course of Action & Summary of Work Done

In order to demonstrate the proposed principles in practice, a high-performance pipeline ADC has been designed and is expected to be fabricated and tested soon. Salient parameters pertaining this ADC are shown in Table 1. A block diagram of the ADC is shown in Fig. 1. The ADC utilizes a highly linear wideband track-and-hold (THA) to achieve a high level of design flexibility. Highly linear amplifiers are used, and these are scaled aggressively to minimize overall power consumption of the circuit in order to achieve the target power consumption. On-chip digital calibration is also utilized in order to remove nonidealities resulting from element mismatch.

Parameter	Target Value
Resolution	16 bits
Accuracy	> 14 bits
Sampling rate	20 Msps
Power consumption	200 mW @ 3.3V supply
Supply voltage	3V-3.6V
Technology	0.35 μm CMOS

Table 1 Salient parameters pertaining the prototype ADC

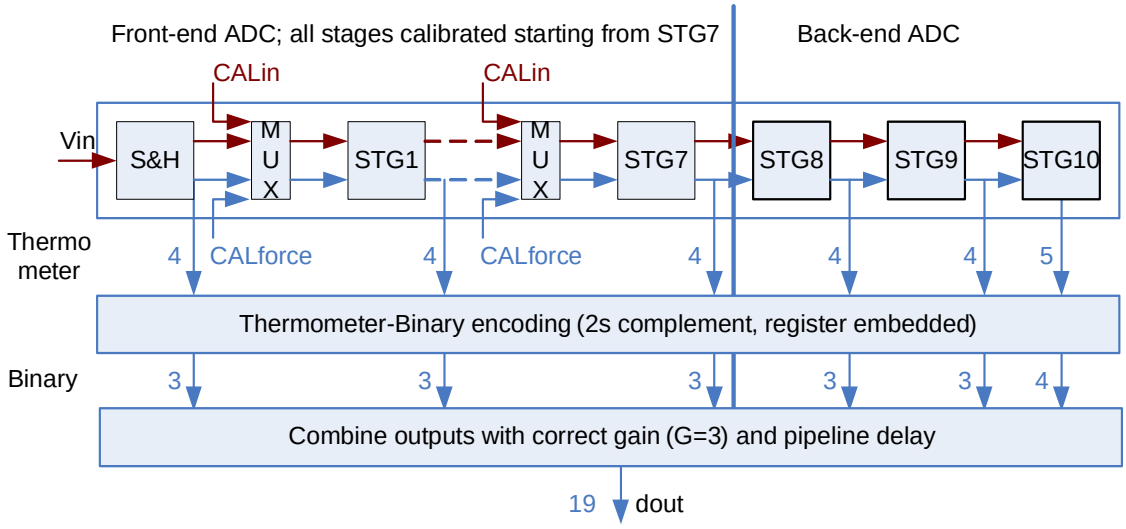

Fig. 1 A block diagram of the proposed ADC. The digital combiner includes a correction for element mismatch to improve linearity of the device. The device features a calibration mode (CAL) in addition to the normal mode of operation in order to allow calibration of various circuit-level nonidealities and their subsequent removal.

The design has been extensively simulated at various levels of abstraction to ensure that the target performance is indeed achievable. In this task, the authors have worked closely with the design foundry (Austriamicrosystems AG) to ensure that various important second-order effects were measured and incorporated into the existing simulation models, particularly short-channel effects relating to lowered gain due to impact ionization, and accurate measurements of short-channel noise behavior in the transistors. New simulation methodologies have been used to validate the performance of the circuits used. As the aim is to develop practical ADC circuits, special attention has been paid to reliability issues. These include yield analysis, electrostatic discharge (ESD) protection and element mismatch. Special circuit-level techniques are used to prevent performance degradation due to element mismatch and electrical overstress (EOS) while achieving a high level of performance in every aspect. The various insights offered by this work coupled with first silicon results should allow further improvements in future design work.

3. Further Directions

The prototype device will be fabricated and tested in Q1 2007. Currently, the prototype device is being prepared for tapeout and fabrication, and test setups are being developed. It is

expected that the first silicon results will be available in March/April 2007. Further work is expected to include detailed description of the formal design technique used to derive critical circuit-level parameters from the system parameters, and a description of various tradeoffs involved in the design procedure.

More advanced versions of the prototype device are expected to be developed, particularly to allow use of double-sampling to achieve a doubling of overall conversion rate. Further higher speed versions of the design utilizing an advanced silicon-germanium (SiGe) BiCMOS process and other circuit design approaches will also be investigated at this time.

4. Acknowledgments

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References

[1] Sharma, V., Moon, U., Temes, G. C., "Generalized Radix Design of Low-Power, High-Performance Pipelined ADCs," *Proc. ISCAS '05*, Kobe, Japan.
[2] Sharma, V., "Generalized Radix Design Techniques for Low-Power, Low-Voltage Pipelined & Cyclic ADCs," M.S. Thesis, Oregon State University, 2004.