Multiplexed Incremental Data Converters for EEG Monitoring and Recording

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Abstract

The purpose of this research was to develop integrated analog-to-digital data converters (ADCs) which are suitable for the simultaneous acquisition of a large number (100 to 300) of electroencephalographic (EEG) signals. These signals are then processed by a computer. The EEG signals have narrow bandwidths, typically around 400 Hz, but their amplitudes are small and they need to be accurately acquired in the presence of high-level noise. This requires a large dynamic range, around 19 bits, for the devices implementing the data conversion. It is also preferable that the complete data acquisition structure be portable, and hence battery powered. This in turn requires low power dissipation by the data converters used.

Sensor arrays detecting EEG signals have been successfully used in the noninvasive location of the sources of epilepsy in the brain [1],[2],[3]. Under this project we have compared the available techniques (one ADC/channel, multiplexed delta-sigma ADCs, shared incremental ADCs) for this application. Using an ADC in each channel provides flexibility, but requires significant power dissipation, and may introduce mismatch effects. Conventional multiplexing of delta-sigma converters reduces power dissipation, but is subject to interchannel interference. Shared incremental data converters need more power than multiplexed delta-sigma ones, but they promise to be highly accurate under the specified conditions [4]. We compared these techniques by simulations, chose the most suitable method, and are currently implementing it by an integrated device. The architectural simulations of the chip are completed, and the transistor-level design is also nearing completion.

In the research, we also discovered an exact analytical technique for the optimal design of the digital signal processing segment of incremental ADCs. A full paper was written, and accepted for publication on this in the IEEE Trans. on Circuits and Systems [8]. It acknowledges the support provided by the Catalyst Foundation.

Introduction

Incremental ADCs are essentially delta-sigma ($\Delta\Sigma$) ADCs which are reset after each conversion. Due to the noise-shaping nature of the high-order $\Delta\Sigma$ modulators, the incremental ADC is much more efficient in conversion time than the dual-slope ADC. Incremental ADCs provide high-resolution A/D conversion for instrumentation and measurement (I&M) as well as biomedical applications.

One of the advantage of incremental ADC is that it can be easily multiplexed (Fig. 1). Due to the limited memory, it is more stable and less tonal than the traditional delta-sigma ADC. It also allows for accurate gain and offset compensation [6].

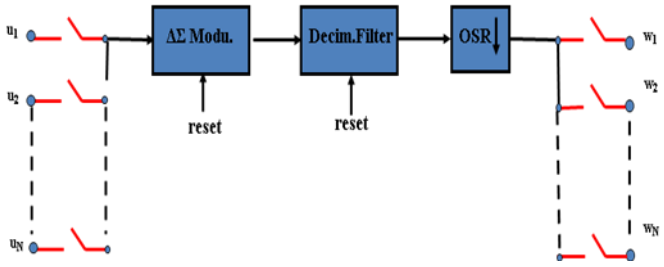


Fig. 1. The block diagram of the multiplexed incremental ADC.

An overview on incremental ADC can be found in [5]. A 22-bit 0.3 mW incremental ADC for DC measurement was reported in [6]. Incremental ADC for wideband application is discussed in [7].

Analysis of the Incremental ADC

We developed a technique for the noise analysis of the incremental ADCs [8]. Due to the reset of the ADC, the impulse response of the signal transfer function (STF) and noise transfer function (NTF) are changed from infinite length to finite length. Suppose the incremental ADC is reset every M clock periods. The final conversion result in the nth conversion cycle can be calculated as follows.

$$v(n) = \left[stf'(k) * u(k)\right]_{M,n} + \left[stf'(k) * t(k)\right]_{M,n} + \left[ntf'(k) * q(k)\right]_{M,n} \quad (1)$$

where *stf'*(*k*) is the first *M* impulse response of the overall signal transfer function *STF*(*z*)*H*(*z*), and *ntf'*(*k*) is the first *M* impulse response of the overall noise transfer function *NTF*(*z*)*H*(*z*). The *STF*(*z*) and *NTF*(*z*) are the signal transfer function and noise transfer function of the ΔΣ modulator without reset. The *H*(*z*) is the transfer function of the decimation filter without reset. The *u*(*k*) is the input signal, *t*(*k*) is the input-referred thermal noise and *q*(*k*) is the quantization noise.

The first, second and third term in (1) represents the signal component, the thermal noise and the quantization noise in the output, respectively. The power of the input-referred thermal noise *t*(*k*) can be estimated by $\gamma kT / C_{in}$, where *k* is the Boltzmann constant, *T* is the absolute temperature and C_{in} is the value of the input capacitors. The constant γ can be estimated from input circuitry (γ=5 is a good choice) [9]. The power of *q*(*k*) is regarded as $\Delta^2/12$, where Δ is the step size of the quantizer.

We denote *stf*(*k*) and *ntf*(*k*) as the first *M* impulse response of *STF*(*z*) and *NTF*(*z*), and *h*(*k*) as the first *M* impulse response of *H*(*z*). These impulse responses are denoted by

$$
\begin{aligned}
stf(k) &= \{s_0, s_1, \cdots, s_{M-1}\} \\
ntf(k) &= \{n_0, n_1, \cdots, n_{M-1}\} \\
stf'(k) &= \{s'_0, s'_1, \cdots, s'_{M-1}\} \\
ntf'(k) &= \{n'_0, n'_1, \cdots, n'_{M-1}\} \\
h(k) &= \{h_0, h_1, \cdots, h_{M-1}\}.
\end{aligned} \tag{2}
$$

Because $stf'(k) = stf(k)*h(k)$ and $ntf'(k) = ntf(k)*h(k)$, the following vector relations hold

$$
\begin{aligned}
\mathbf{s}' &= \mathbf{S} \cdot \mathbf{h} \\
\mathbf{n}' &= \mathbf{N} \cdot \mathbf{h}
\end{aligned} \tag{3}
$$

where

$$
\begin{aligned}
\mathbf{s}' &= \left[s'_0, s'_1, \cdots, s'_{M-1}\right]^T \\
\mathbf{n}' &= \left[s'_0, s'_1, \cdots, s'_{M-1}\right]^T \\
\mathbf{h} &= \left[h_0, h_1, \cdots, h_{M-1}\right]^T \\
\mathbf{S} &= \begin{bmatrix} s_0 & 0 & 0 & \cdots & 0 \\ s_1 & s_0 & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ s_{M-1} & s_{M-2} & s_{M-3} & \cdots & s_0 \end{bmatrix} \\
\mathbf{N} &= \begin{bmatrix} n_0 & 0 & 0 & \cdots & 0 \\ n_1 & n_0 & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ n_{M-1} & n_{M-2} & n_{M-3} & \cdots & n_0 \end{bmatrix}.
\end{aligned} \tag{4}
$$

From (1) to (4), the thermal noise power can be estimated by

$$
\begin{aligned}
\overline{v_t(n)^2} &= \frac{\gamma kT}{C_{in}}\left(s_0'^2 + s_1'^2 + \cdots + s_{M-1}'^2\right) \\
&= \frac{\gamma kT}{C_{in}}\mathbf{h}^T \cdot \mathbf{S}^T \cdot \mathbf{S} \cdot \mathbf{h}.
\end{aligned} \tag{5}
$$

The quantization noise power can be estimated by

$$
\begin{aligned}
\overline{v_q(n)^2} &= \frac{\Delta^2}{6}\left(n_0'^2 + n_1'^2 + \cdots + n_{M-1}'^2\right) \\
&= \frac{\Delta^2}{6}\mathbf{h}^T \cdot \mathbf{N}^T \cdot \mathbf{N} \cdot \mathbf{h}
\end{aligned} \tag{6}
$$

Suppose the maximum peak-to-peak output sine wave amplitude is V_{pp}. The SNR of the incremental ADC is

$$
SNR = 10\log\left[\frac{V_{pp}^2/2}{\overline{v_t(n)^2} + \overline{v_q(n)^2}}\right] = 10\log\left[\frac{V_{pp}^2/2}{\mathbf{h}^T \cdot \mathbf{O} \cdot \mathbf{h}}\right] \tag{7}
$$

where

$$\mathbf{O} = \frac{\gamma kT}{C_{in}}\left[\mathbf{S}^T \cdot \mathbf{S} + \rho \cdot \mathbf{N}^T \cdot \mathbf{N}\right] \tag{8}$$

and

$$\rho = \frac{\Delta^2 / 6}{\gamma kT / C_{in}}. \tag{9}$$

SNR Optimization

Based on the above analysis, we proposed a SNR optimization technique [8]. The overall noise is minimized for a given power consumption by choosing *M*, C_{in} and the impulse response of the decimation filter $h(k)$ properly.

For a given *M* and C_{in}, the optimization of the impulse response of the decimation filter can be formulated as follows.

$$\begin{aligned} &\min \mathbf{h}^T \cdot \mathbf{O} \cdot \mathbf{h} \\ &s.t. \mathbf{e}^T \cdot \mathbf{h} = 1 \end{aligned} \tag{10}$$

where **O** is defined in (8) and **e** is the $[1,1,\cdots,1]^T$. The objective function is the overall noise and the constraint is to ensure $H(z) = 1$ for $z = 1$. Since $STF(z)$ is 1, the constraint ensures the overall signal transfer function to be 1 at DC.

The quadratic programming (10) can be solved with Matlab. The analytical solution can also be found by Lagrange multiplier technique [8] as

$$\mathbf{h}^* = \frac{\mathbf{O}^{-1}\mathbf{e}}{\mathbf{e}^T\mathbf{O}^{-1}\mathbf{e}}. \tag{11}$$

It is observed that the optimal **h** for thermal noise only is $\mathbf{h}^*_{thermal} = \left[\frac{1}{M}, \frac{1}{M}, \cdots, \frac{1}{M}\right]^T$. When the quantization noise is taken into account, the optimal **h** turns into $\mathbf{h}^*$. We define the *thermal noise penalty factor* as

$$\beta = \frac{\text{actual thermal noise power}}{\text{minimum thermal noise power}} = \frac{\sum_{i=0}^{M-1} 1/h_i^{*2}}{\sum_{i=0}^{M-1} 1/M^2}. \tag{12}$$

The typical value of β is around 1.5. It reflects the trade-off between the thermal noise and quantization noise.

System Design

The design specification is listed in Table I.

TABLE I
DESIGN SPECIFICATION FOR THE INCREMENTAL ADC

Specifications	Value
Number of channels (N)	20
Signal bandwidth (f_b)	3 kHz
Signal-to-noise ratio (SNR)	$\geq$ 100 dB
Maximum output signal power (V_{max}^2)	1 V^2
Maximum sampling (f_c)	30 MHz

The design procedures are given as follows.

Step 1. Calculate the maximum conversion time for one channel: $T_w = 1/(2Nf_b) = 8.33$ μs.

Step 2. Calculate the maximum clock cycles for one conversion: $M_{max} = T_w f_c = f_c /(2Nf_b) = 250$.

Step 3. A third order ΔΣ modulator with a 5-level quantizer [10] is designed with the delta-Sigma toolbox for Matlab [11] (Fig. 2). The NTF of the modulator is $NTF = \dfrac{(z-1)^3}{(z-0.5701)(z^2-1.39z+0.6149)}$ and the STF is 1.

Step 4. Determine the minimum value of MC_{in}. Since the SNR needs to be larger than 100 dB, the maximum total noise power is $P_{tot} = 10^{-10}$ V^2. If we allocate 90% of the noise budget to the thermal noise, the thermal noise must satisfy $\dfrac{\gamma kT\beta_{\max}}{MC_{in}} \leq 0.9P_{tot}$, where $\beta_{\max} = 2$ [8]. This gives $MC_{in} \geq 460\text{pF}$.

Step 5. Determine M and C_{in}. A series of optimizations for different M and C_{in} show that larger M and smaller C_{in} gives better SNR. However, M is limited by the M_{max} calculated in *Step 2*. For our design, we choose M = 230 and C_{in} = 2 pF.

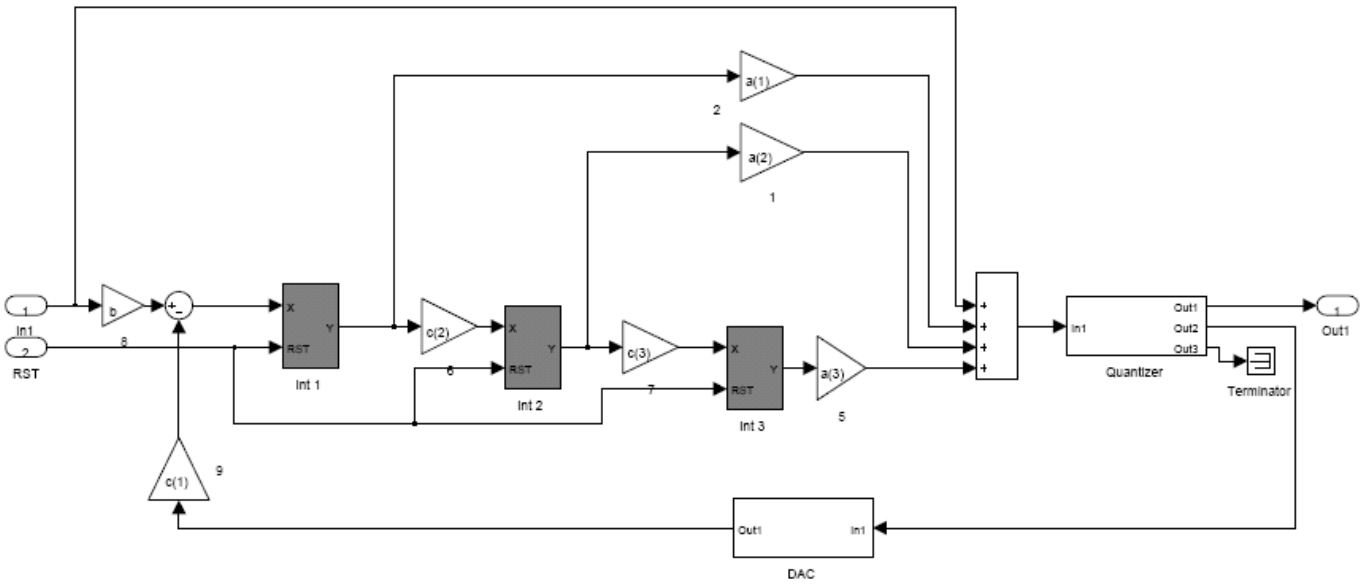


Fig. 2. A third order ΔΣ modulator with a 5-level quantizer.

Step 6. Optimize the decimation filter by solving (10). The impulse response of the optimal decimation filter is shown in Fig. 3. The output thermal noise and quantization noise are expected to be −103 dBFS and −115 dBFS, respectively.

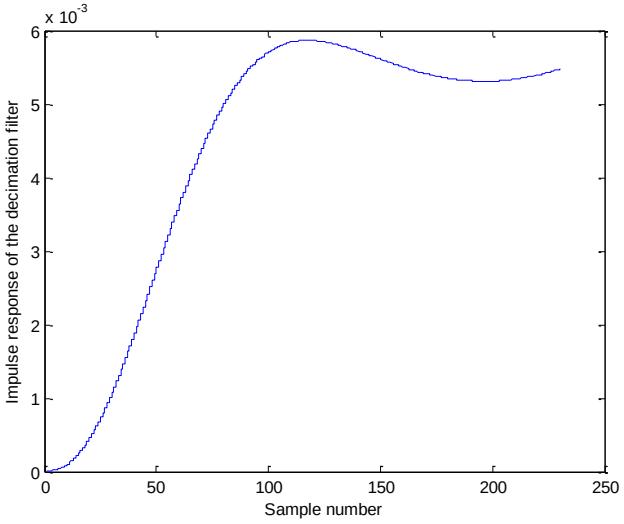


Fig. 3. The impulse response of the optimal decimation filter.

Dynamic Range Scaling

As shown in Fig. 4, the output of the 3rd integrator exceeds the desirable opamp output swing. So dynamic scaling is performed by the delta-sigma toolbox for Matlab [11].

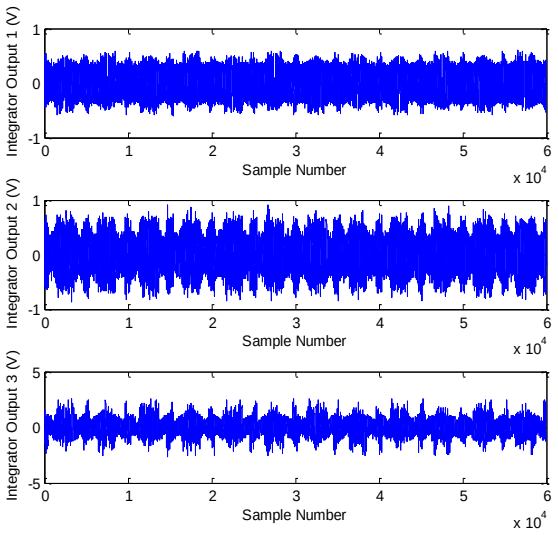
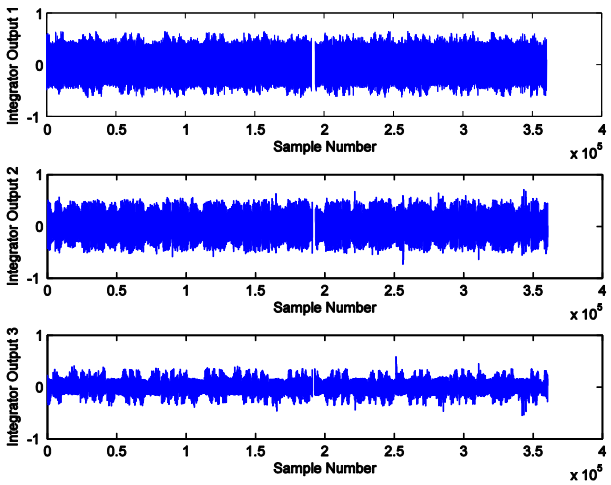


Fig. 4. The integrator outputs for a 0.5 V amplitude, 3 kHz sinusoidal input. The reference voltage is 1 V. The output of the third integrator exceeds the reference voltage.

The integrator outputs for the delta-sigma modulator after scaling are shown in Fig. 5. After the dynamic scaling, the coefficients of delta-sigma modulator are given as follows.

$$\mathbf{a} = [0.9831, 0.7850, 0.7151]^T$$
$$\mathbf{b} = [1.0577, 0, 0, 1.0000]^T$$
$$\mathbf{c} = [1.0577, 0.5865, 0.2179]^T .$$



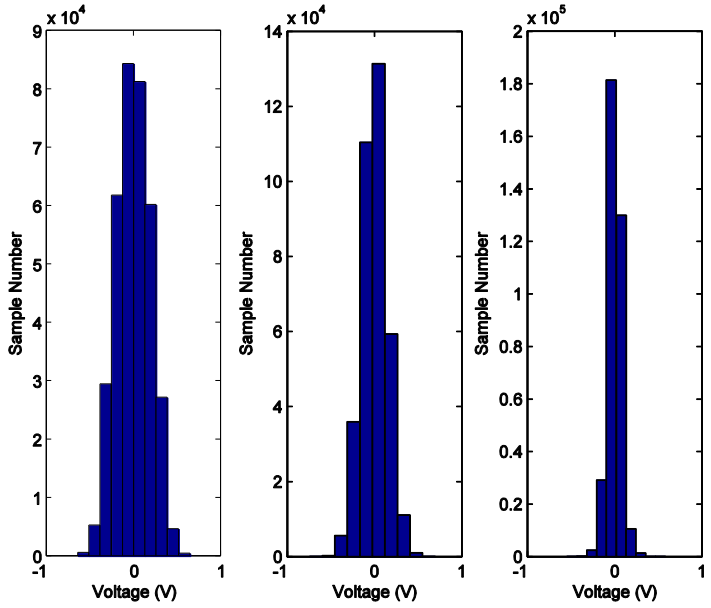


Fig. 5. The input is 507 Hz, -1 dBFS sine wave. The reference voltage is 1 V. All integrator outputs are below 1 V. For 1.8 V reference voltage, the opamp output swing is ±1.8*0.65 = ±1.17 V (0.3–1.5 V).

MATLAB Simulation

For ideal integrators, the conversion error versus the DC input level is shown in Fig. 6. The dash and dotted line shows the theoretical prediction for the thermal noise and the quantization noise, respectively.

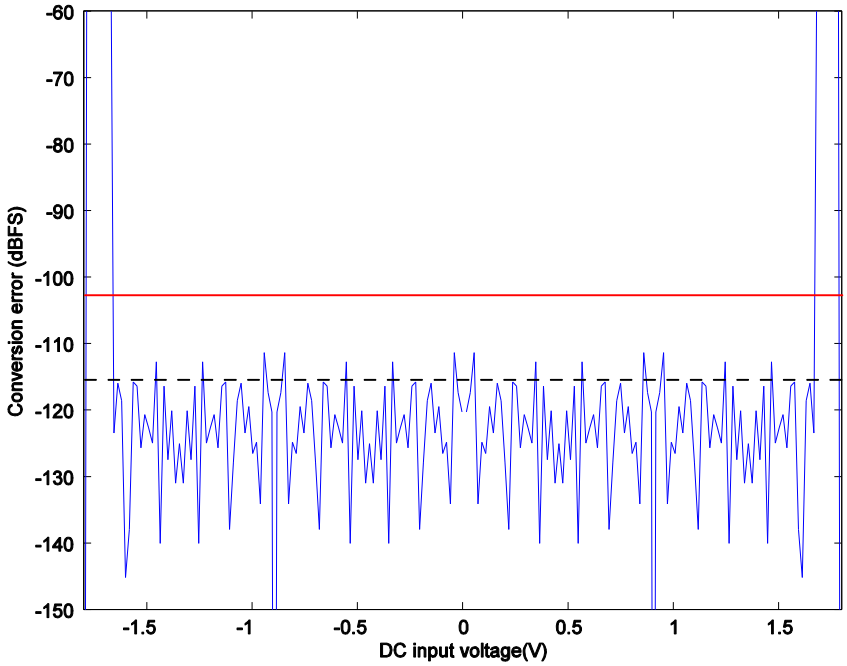


Fig. 6. The conversion error versus the DC input level for ideal integrators.

The SQNR versus the sine wave input amplitude (507 Hz) is shown in Fig. 7.

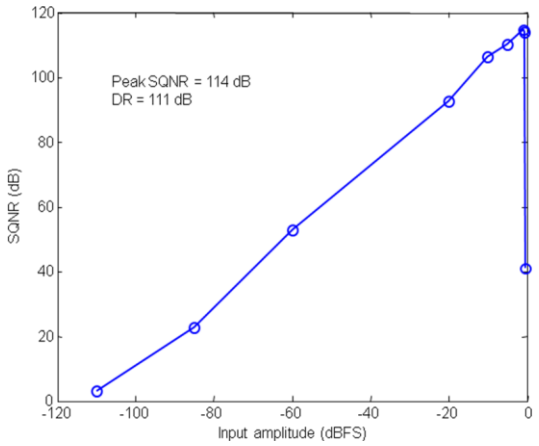
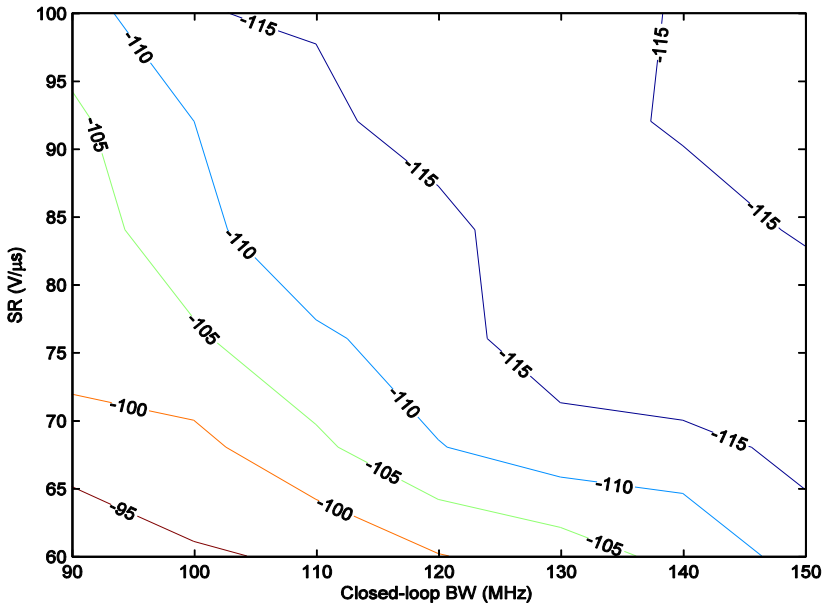
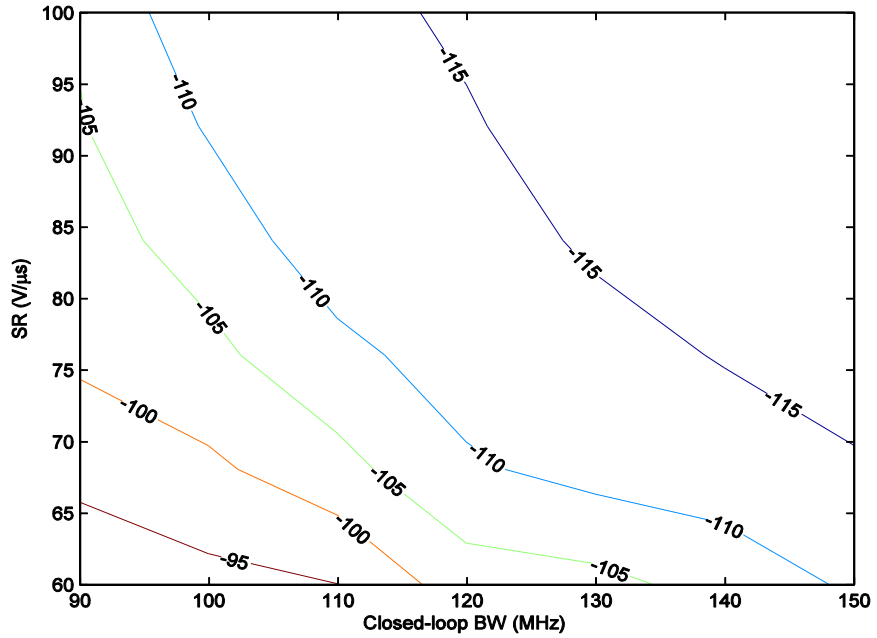


Fig. 7. SQNR versus input sine wave amplitude.

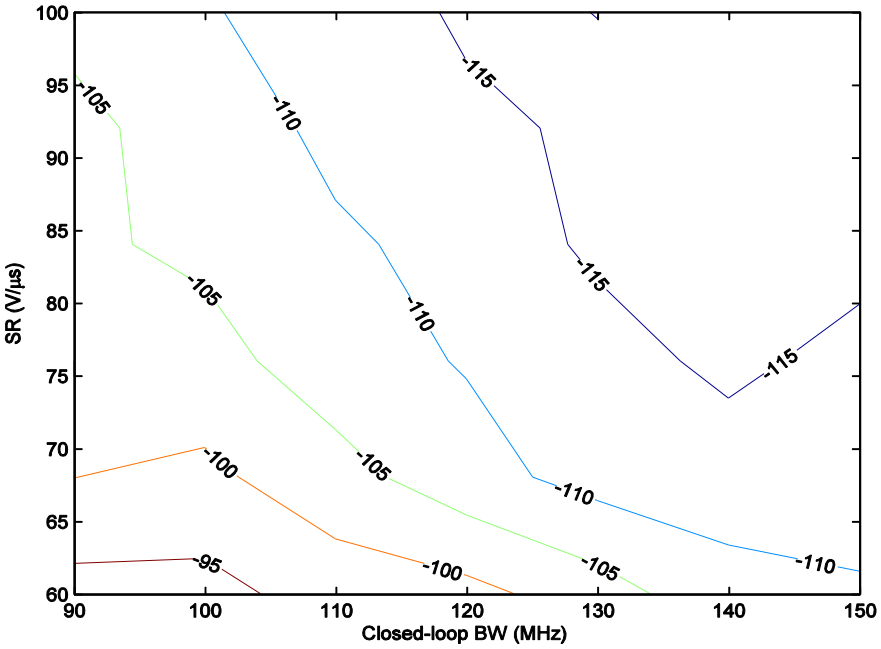
The effect of non-ideal integrator is simulated with SD Toolbox 2 [12]. The average conversion error between -0.75 V and 0.75 V versus the DC gain, the GBW and the SR are shown in Fig. 8.



a)



b)



c)

Fig. 8. The average conversion error in dB between -0.75 V and 0.75 V versus the closed-loop GBW and the SR for a) 70 dB, b) 60 dB and c) 50 dB DC gain.

Based the simulation results, the opamp specifications are shown in Table II. The corresponding DC sweep result is shown in Fig. 9.

TABLE II
OPAMP SPECIFICATIONS

Specifications	1st stage	2nd stage	3rd stage
DC Gain	60 dB	50 dB	50 dB
Closed-loop BW	115 MHz	70 MHz	46 MHz
SR	80 V/μs	48 V/μs	32 V/μs
Output Swing	0.3 V – 1.5 V	0.3 V – 1.5 V	0.3 V – 1.5 V
Supply Voltage	1.8 V	1.8 V	1.8 V

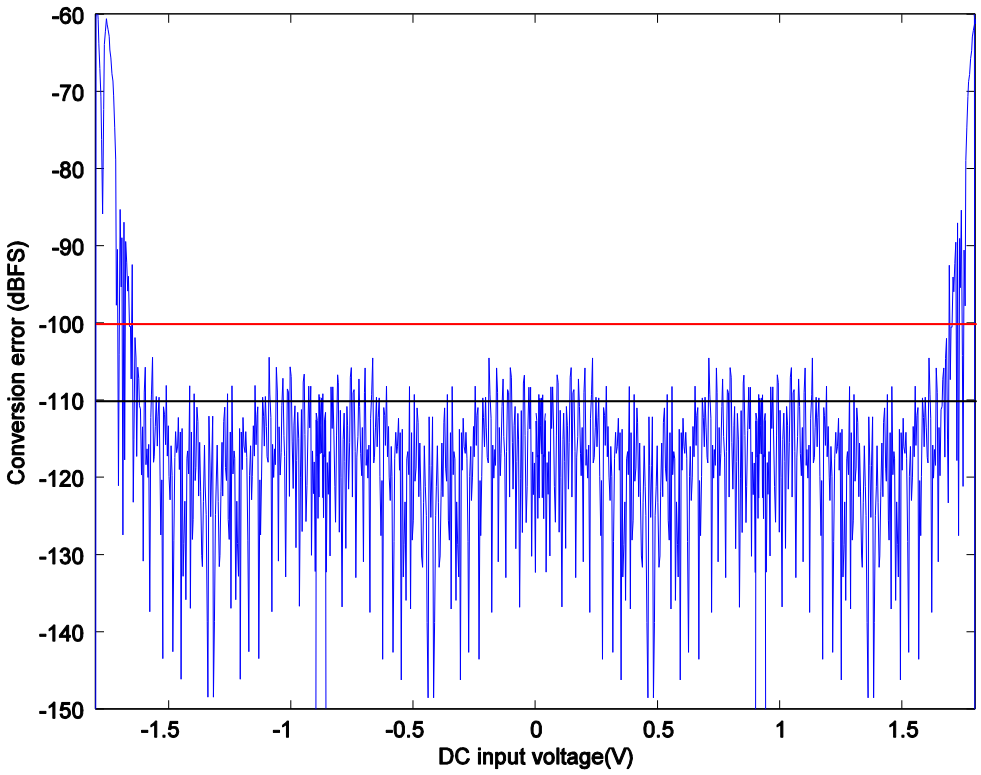


Fig. 9. The conversion error versus the DC input level with opamp non-idealities shown in Table II.

The maximum steps of the 1st, 2nd and 3rd integrators for a -1 dBFS 507 Hz sine-wave input are determine to be 0.65, 0.50 and 0.28, respectively. For 1.8 V reference, the maximum steps (differentially)

are 1.17 V, 0.9 V and 0.5 V, respectively. We allow 20 % of one clock phase for the slewing, *i.e.*, 3 ns. Thus the slew rates (differentially) for the 1st, 2nd and 3rd opamps are 390 V/μs, 300 V/μs and 93 V/μs. The revised specifications are summarized in Table III.

TABLE III
OPAMP SPECIFICATIONS

Specifications	1st stage	2nd stage	3rd stage
DC Gain	60 dB	50 dB	50 dB
Closed-loop BW	115 MHz	70 MHz	46 MHz
SR	390 V/μs	300 V/μs	93 V/μs
Output Swing	0.3 V – 1.5 V	0.3 V – 1.5 V	0.3 V – 1.5 V
Supply Voltage	1.8 V	1.8 V	1.8 V

Switch-Cap Realization – Behavior Model Simulation

The switch-cap circuit of the delta-sigma modulator is shown in Fig. 10. The behavior model of opamp is shown in Fig. 11. The behavior model of the 5-level quantizer is implemented by Verilog-A. The power supply and the reference voltages are 1.8 V.

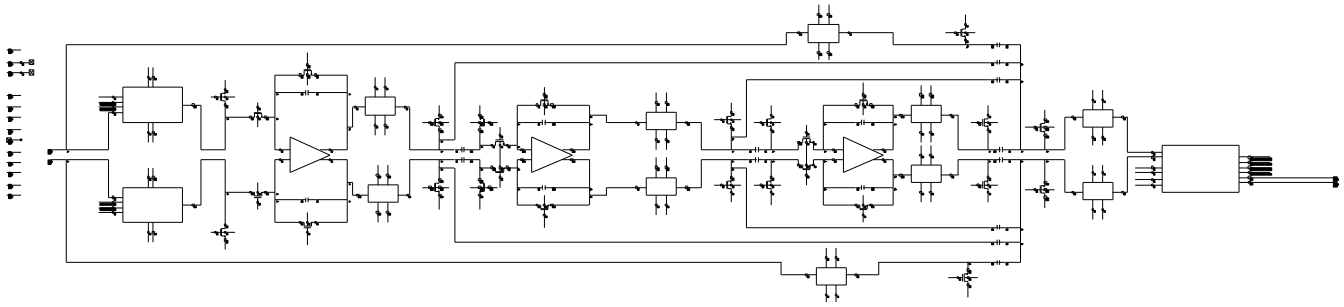


Fig. 10. The circuit schematic of the delta-sigma modulator

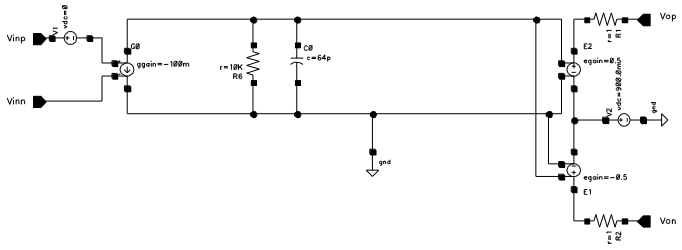


Fig. 11. The opamp model.

The unit circuit of the switch-cap DAC is shown in Fig. 12. The whole DAC consist of four units controlled by four digital bits fed back from the quantizer. The input sampling cap is shared between the input branch and the DAC feedback branch. A bootstrap switch is used for sampling the signal.

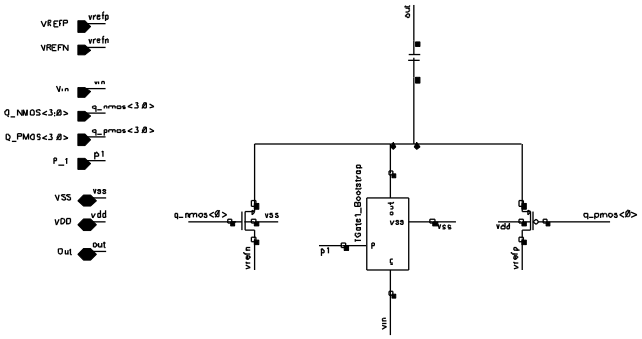
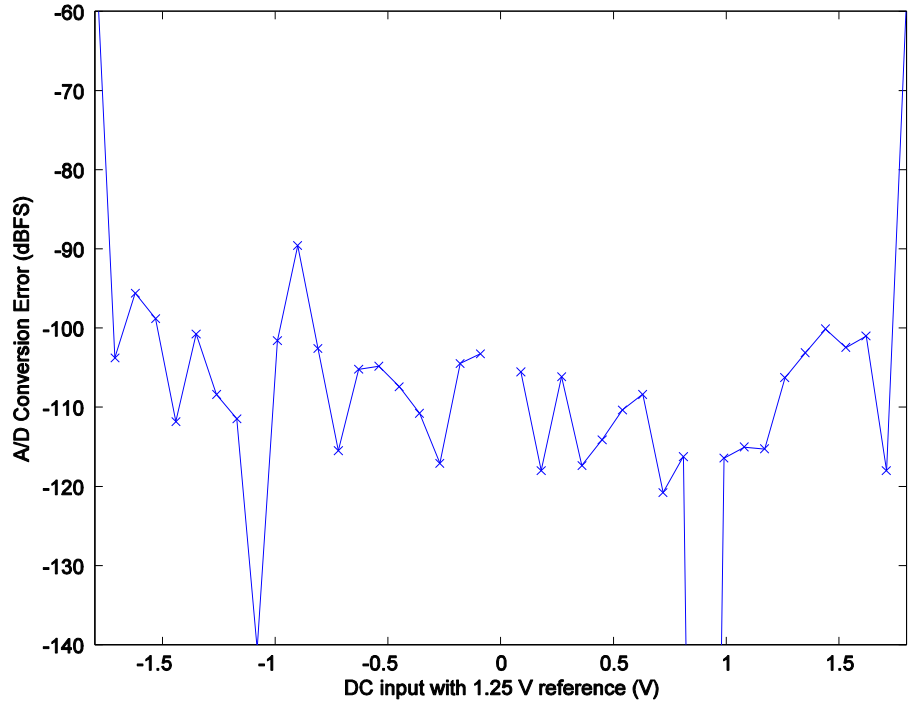


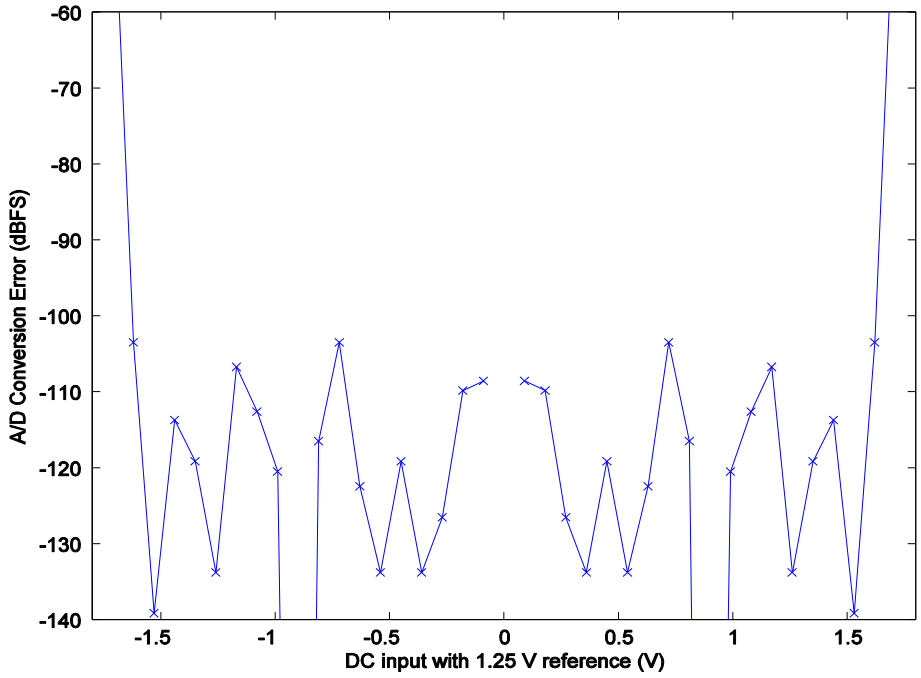
Fig. 12. The schematic of the DAC (one unit).

For the first integrator, if we choose $f_{UGBW\_CL}=140\text{MHz}$ and $R=90\Omega$, we can calculate that [14] $f_{UGBW\_CL,R}=\dfrac{f_{UGBW\_CL}}{1+2\pi\cdot f_{UGBW\_CL}RC_S}=121\text{MHz}$, which satisfies the specification in Table II.

As shown in Fig. 13, the conversion error versus DC input voltage are obtained through simulations, with ideal switches (Verilog-A model) and real CMOS switches.



a)



b)

Fig. 13. The conversion error versus DC input voltage with a). CMOS switches with 0.18 μm National CMOS9 model and b). ideal switches.

Opamp Design

As shown in Fig. 14, a gain-boosting folded-cascode opamp is designed for the first integrator.

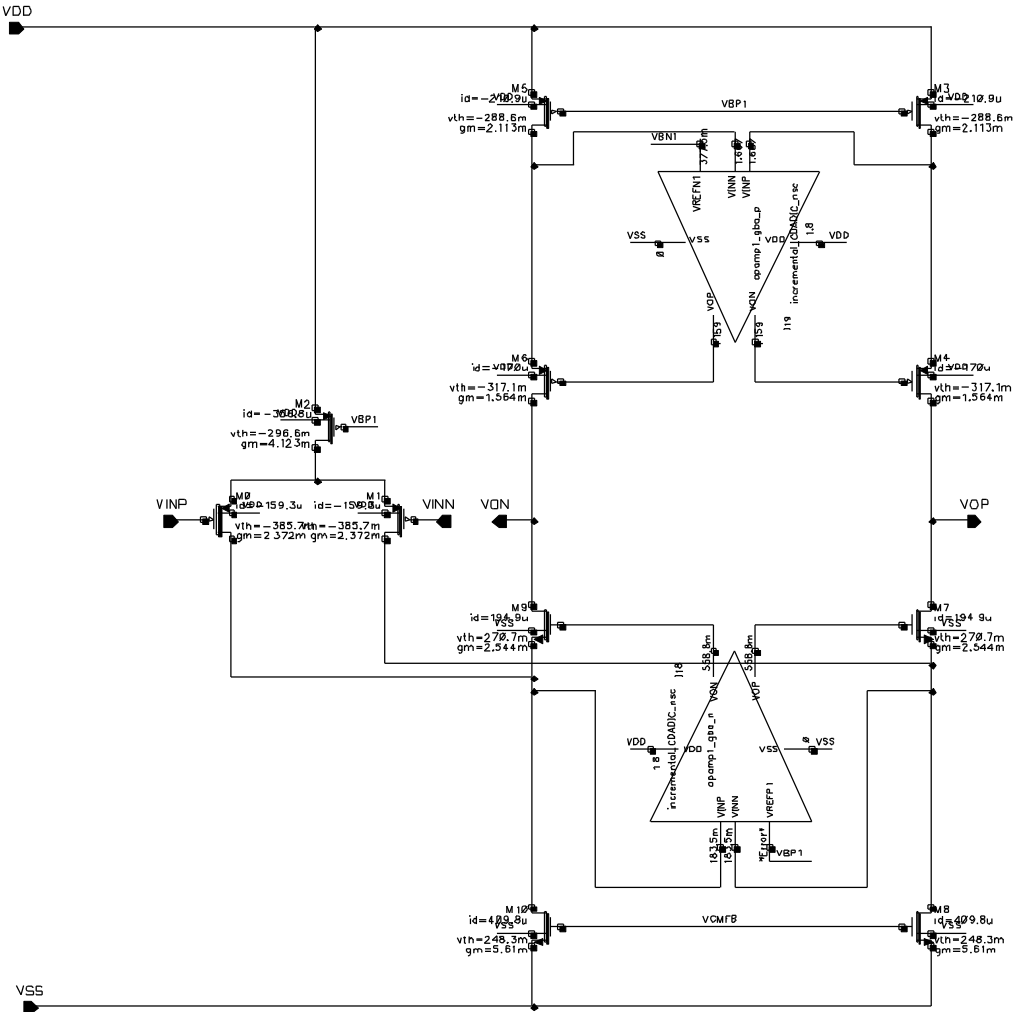


Fig. 14. The opamp for the first integrator.

The performance of the opamp is summarized in Table IV.

TABLE IV
THE OPAMP PERFORMANCE (1ST INTEGRATOR)

Parameter	Value	Specification
DC gain	64 dB	60 dB
Closed-loop BW	131 MHz	115 MHz
Output Swing	0.3 V – 1.5 V	0.3 V – 1.5 V
Slew Rate	400 V/μs	390 V/μs
Power Consumption	2 mW	–

Correlated Double Sampling

Correlated double sampling (CDS) is used in the first integrator to reduce the DC offset and the 1/f noise of the opamp. The schematic [15] is shown in Fig. 15. The simulation of the CDS integrator is in progress.

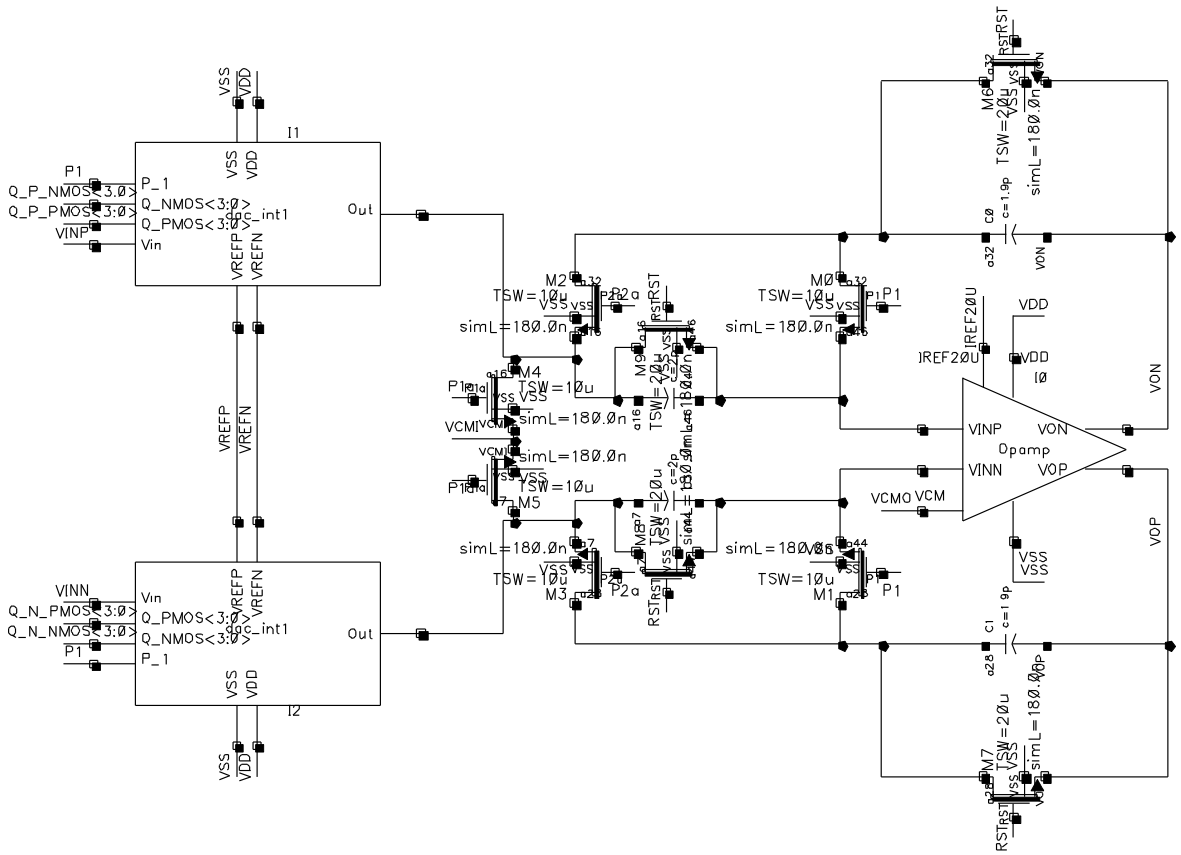


Fig. 15. The CDS integrator (1st integrator).

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