Research on Electronic Cytosensors
Progress Report for 2003

Project supported by

Catalyst Foundation

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26th November, 2003

Introduction

The purpose of this research is to develop biological sensors, which can detect biohazardous conditions. The main effort (by Profs. Moon & Temes and students Rengachari & Sharma) is to investigate the electronic aspects of the sensor; the second (by Prof. Chaplen & his students) provides the biochemical support by supplying cells, chemicals and by advising on testing, data analysis and capture.

The main results obtained thus far are described in this report, along with a roadmap for future research. After a number of false starts, a suitable sensing mechanism was developed (for details, please refer to last year's annual report [1]). Since then, the focus of our research has been to develop the electronics involved in the sensing process.

Background

Our objective is to develop electronic cytosensors. These are special sensors, which use biological elements to detect or measure biological or chemical agents of interest. They are particularly useful in assessing the hospitability of the environment and the presence of toxic agents. We are looking for generic sensors because our interest is not so much in knowing the exact content of a sample but only in knowing if it is suitable for living organisms. These can be used in a number of fields, including toxicology, pharmacology, medical diagnostics, environmental monitoring, or scientific discovery, where the task might range from detection of contaminants in the water supply to the detection of poisonous gases in a mine. We have added constraints of low cost and portability to the task, and propose to develop cheap, handheld devices.

The above constraints mandate the development of a low-power, low-cost solution in form of an integrated circuit which can be combined with the other elements to yield a compact system.

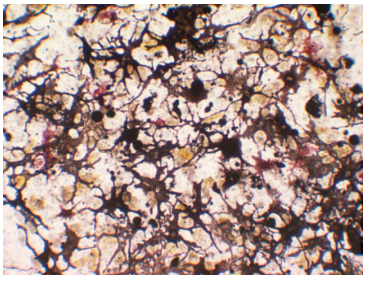

Fig. 1 Chromatophores in hospitable environment

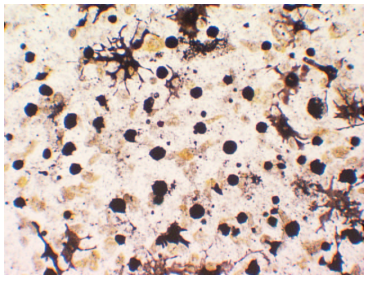

Fig. 2 Chromatophores in hostile environment

Previous Research

A cytosensor was invented by researchers at OSU, which detects the presence of bioactive agents by monitoring changes in the morphology of chromatophores, pigment cells that are known to be highly sensitive to various contaminants and environmental factors. An automated visual inspection method was developed based on observing these changes. When exposed to toxic agents or unfavorable environments, these cells show appreciable change in their appearance, and tend to "aggregate" (Figs.1,2). The aggregation is caused by movement of the pigment cells or chromatosomes along the microtubular skeleton inside the cells. This behavior is typically exhibited in response to environmental stress. These cells are observed through cameras, and any change in their shape is detected using a sophisticated image-processing program. This approach, although successful, requires a lot of equipment and computation, thus rendering it unsuitable for portable applications, and making it costly.

We had proposed a much simpler method based on optical detection in our report last year [1]. Essentially, we obtain an estimate of aggregation induced by an agent by looking at the change in effective cell area. This is done by illuminating the cells, and measuring the intensity of the light transmitted through the sample using a photodiode. As aggregation sets in, the effective area reduces, and the output current goes up. The rate of aggregation can also be measured by observing the output, and different measures can be used for quantifying toxicity, which include the rate of aggregation, and the amount of aggregation observed in the cell sample. One must keep in mind, however, that the cell area itself does not change. It only seems so because of aggregation of chromatosomes inside the cell, and the cytoplasm being essentially transparent, the cell seems to "shrink" in area as a whole, when observed visually or through an optical sensor.

In the comparison between Figs 1 and 2, the latter exhibits a higher signal level, which can be used as an indication of aggregation behavior. A block diagram of the proposed system is shown in Fig. 3. The photocurrent is amplified by a low-noise amplifier, and digitzed by an ADC. The threshold used for detection is set for each new cell sample during a calibration phase.

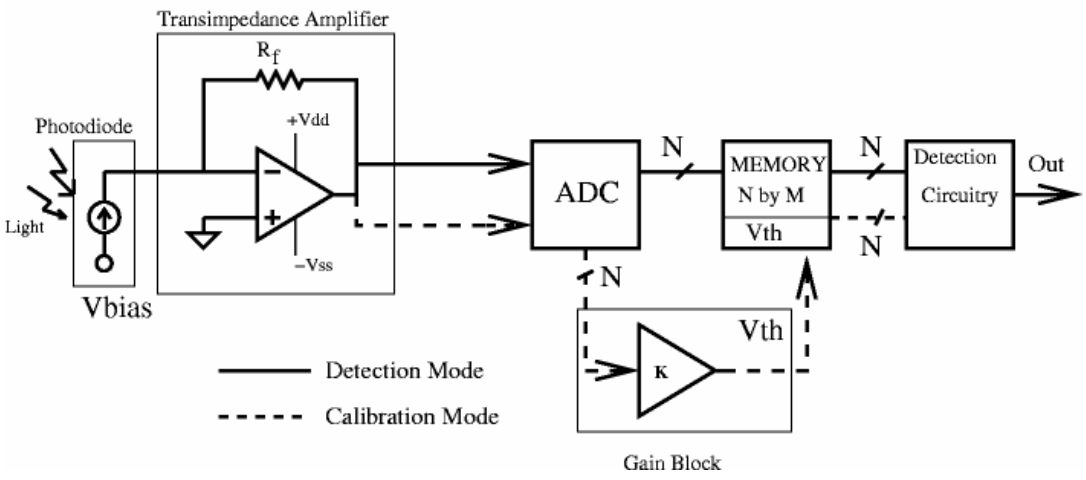

Fig. 3 Electrical representation of the entire system

Once the threshold is set, the system switches to the detection mode. The threshold information and the data obtained during detection can be stored in a small memory and used for post-processing.

Experimental trials involving several different agents confirmed our hypothesis, thus proving the feasibility of this technique. Sample results are shown in Figs.4,5. Each of the curve represents the photocurrent change in a new cell sample, after introduction of an agent. One can see that the photocurrent shows a significant change (>20-25 % of initial value) due to aggregation. Control experiments do not show such trends. This indicates the possibility of choosing a threshold as a ratio of the initial photocurrent reading, and performing detection with the help of a simple electronic system, requiring no human observation.

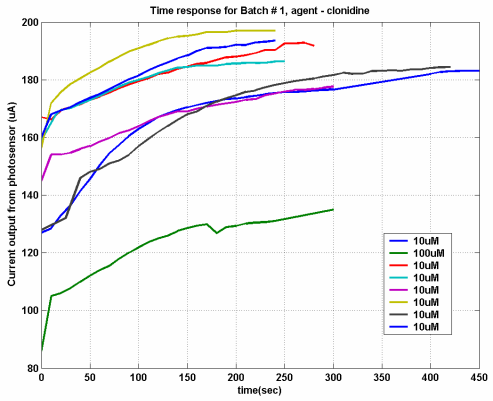

Fig. 4 Experimental results with clonidine

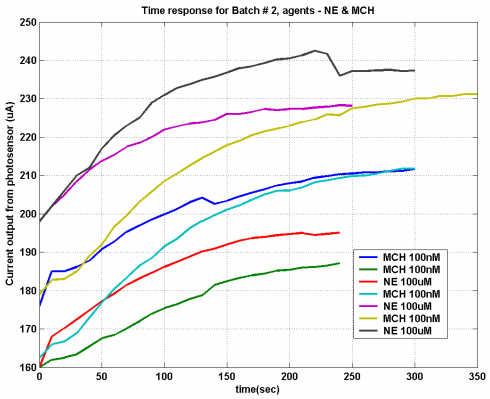

Fig. 5 Experimental results with NE & MCH

An important point is that aggregation is not always the observed reaction to hostile environments. Some cases might exhibit the opposite behavior or no behavior. In addition, some cases of aggregation may occur in perfectly benign conditions. However, by and large, one does observe aggregation in chromatophores as a response to hostile conditions. However, in order to increase the efficiency of this technique, we need to conduct several field trials with various agents and choose an optimal threshold so as to minimise the probability of false alarm, and the probability of failed detection.

Summary of Research

Following the development of a sensing scheme, the next step in our work was to develop the necessary electronics required for analysis and detection of the signal from the photodiode. Once again, the key constraint was to design a low-power, low-cost electronic solution, which prompted us to look for a design comprising CMOS integrated circuits combined together with the photodetector and the cells in a compact system.

The important issue here is to realize low-power implementations of the analog-digital converter, and the low-noise amplifier. Owing to the sensitive nature of the latter, the possibility of reducing it's power consumption is limited and can be achieved primarily by operating the active elements at the lowest power possible without compromising accuracy. The bulk of our research effort was thus focused on designing an energy-efficient ADC suitable for our application.

An Overview of Various ADC Architectures

ADCs come in several flavors, each suited for a different application. Since our application requires a one-one correspondence between input and output, we restrict ourselves to Nyquist-rate ADCs. These are sub-divided further based on the speed and accuracy of conversion, and hardware complexity. A comparison is shown in Table 1.
A detailed description of all these different ADC schemes can be found in [3],[4].

Incremental	Successive Approximation	Algorithmic
High resolution (16~24b)	Medium Accuracy (8~16b)	Medium Accuracy (8~16b)
Very slow	Medium speed	Medium speed
1 bit DAC	Accuracy limited by DAC (multi-bit needed)	1 bit DAC
Simple implementation	Relatively more complex	Simplest implementation
Complex digital filtering required for higher order	Not needed	Not needed
Requires no calibration	Requires extensive calibration for higher resolution	Requires some calibration for higher resolution
Low power consumption	Relatively high power consumption	Lowest power consumption

Table 1 Comparison of different ADC architectures

Based on our system requirements (moderate resolution/speed, low power), we chose the algorithmic scheme for our ADC. To improve performance further, we investigated the possibility of finding new ADC architectures allowing operation at lower power levels than existing algorithmic ADC schemes. Our work yielded a new binary algorithmic ADC architecture capable of operating at lower power levels while achieving accuracy comparable to or better than rival schemes. This ADC was implemented on silicon (details in next section) and test results are awaited.

Implementation Details & Issues

New algorithmic ADC architecture

The new algorithmic ADC architecture (1 bit/stage) is shown in Fig. 6. This is similar to the classical 2-stage pipeline architecture known as the “Nagaraj structure”. A detailed comparison of the two schemes will be presented shortly, and this should illustrate the superiority of the proposed approach. However, first we make a slight modification to the design moving from a 1-bit/stage to a 1.5-bit/stage approach for reasons summarized below.

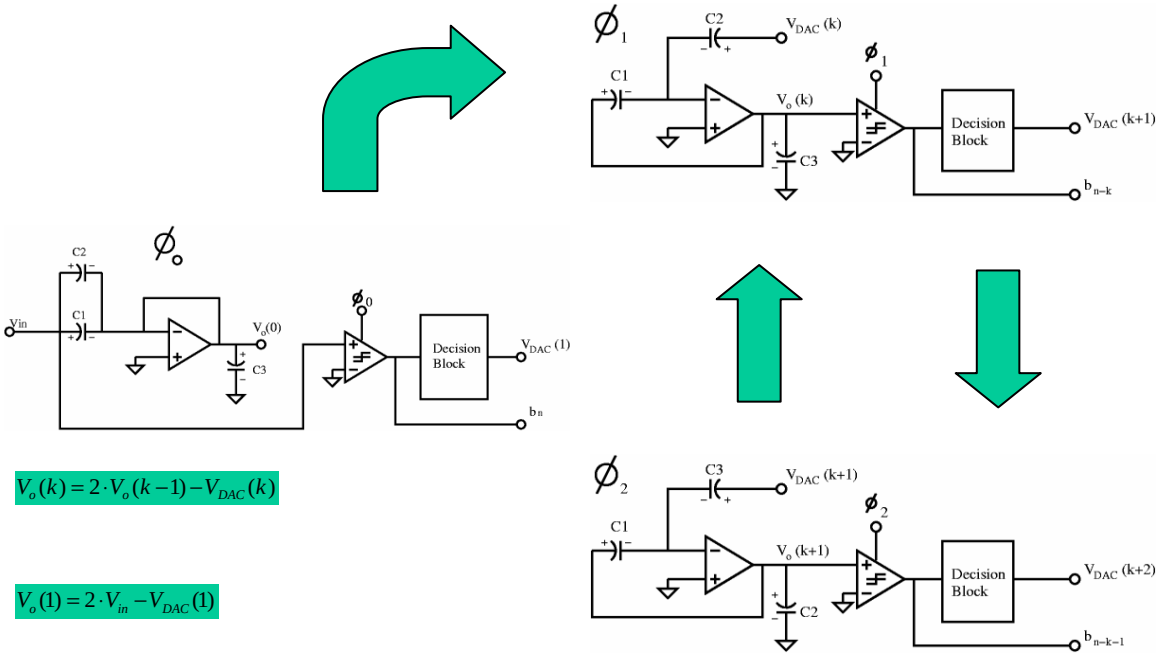

Fig. 6 Proposed architecture for algorithmic ADC in 1-bit/stage implementation

The output V_0 of the opamp recirculates all the while, and is known as the residue. The residue transfer characteristic for the 1-bit/stage scheme is shown in Fig.7. One can see that this scheme is very sensitive to comparator offset, and this makes it hard to use a simple, low-power comparator. However, a slight modification to this scheme makes it much more rugged, and this is shown in Figs 9-10. This scheme known as the 1.5-bit/stage is the *de facto* standard for pipelined and algorithmic ADCs owing to it's tolerance to comparator offsets, ($<V_{REF}/4$). The rival scheme from Nagaraj *et al* is also implemented in the 1.5-bit/stage format (Fig.8).

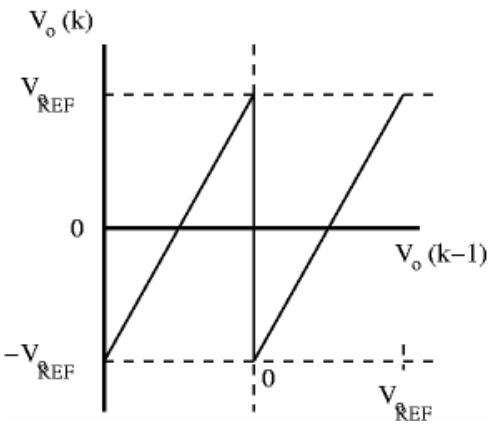

Fig. 7a Residue characteristic without comparator offset

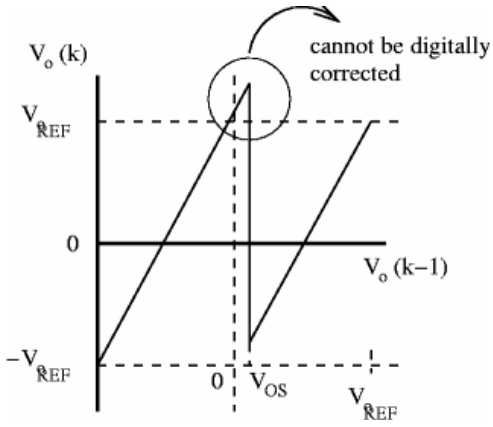

Fig.7b Residue characteristic with comparator offset

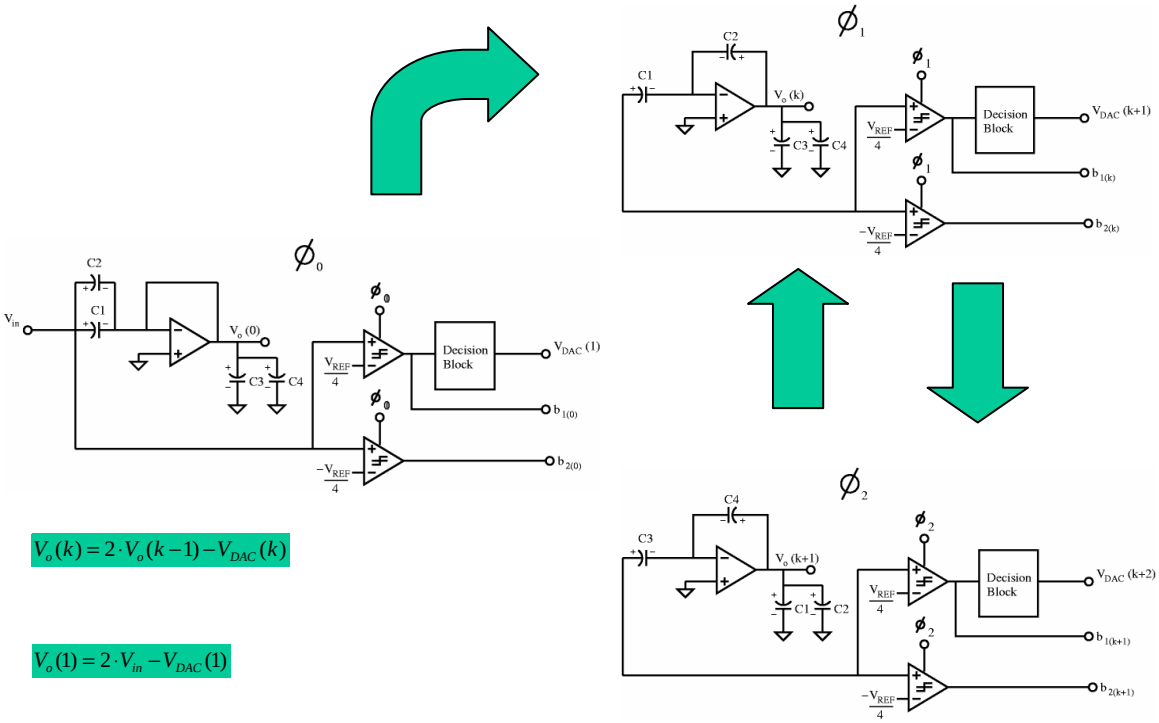

Fig. 8 Nagaraj technique for an algorithmic ADC in a 1.5-bit/stage implementation

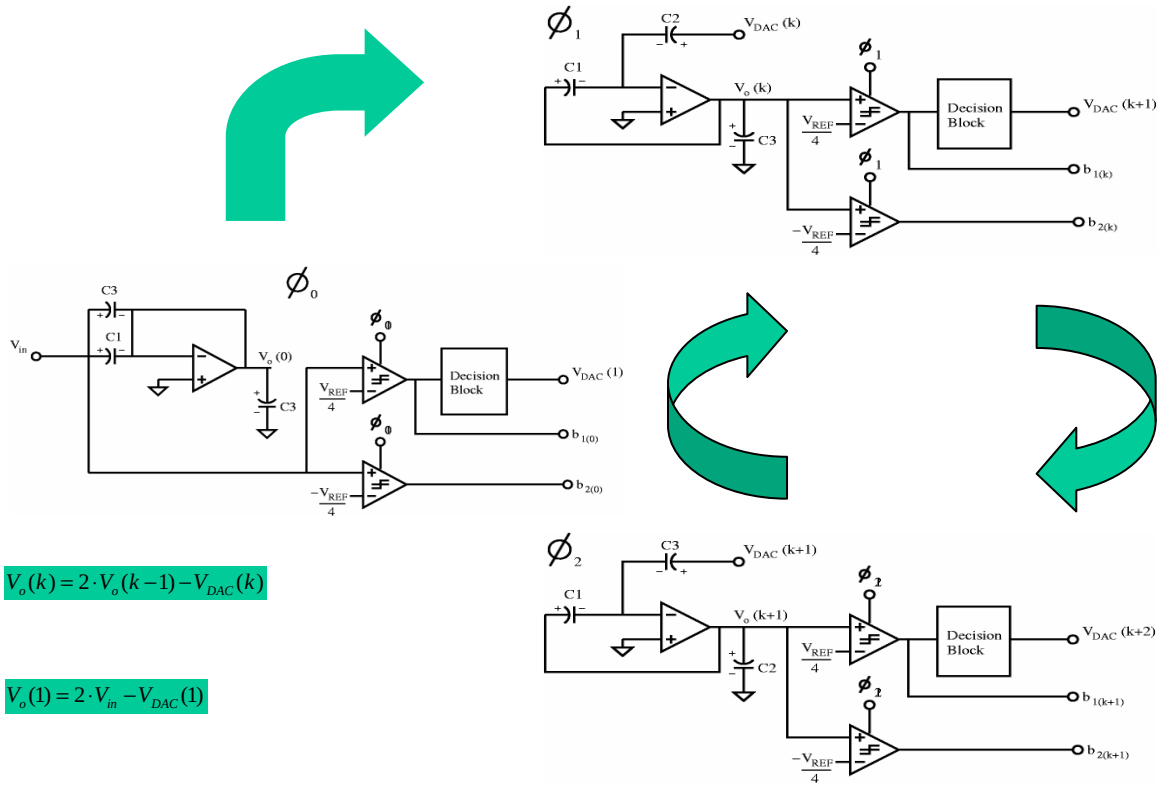

Fig. 9 Proposed algorithmic ADC architecture in a 1.5-bit/stage implementation

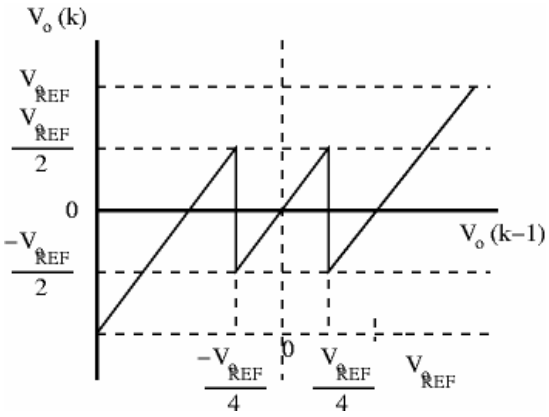

Fig. 10a Ideal residue characteristic for 1.5-bit/stage

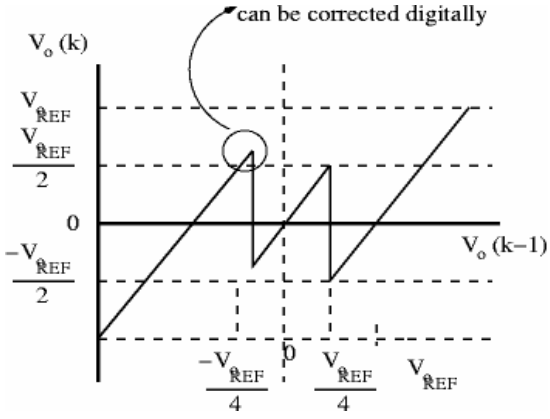

Fig.10b Residue characteristic with comparator offset

One can see that the 1.5-bit/stage scheme is more tolerant to offset. Also, the core of the ADC scheme does not change much, except for a migration from 2 to 3 levels for V_{DAC} and a difference in comparator thresholds. The scheme is known as 1.5-bit because the resolution it provides is 1.5 bits. The 2 comparator outputs are not entirely independent and it is this redundancy that allows us to correct for errors introduced due to comparator offsets. This is demonstrated in Fig. 11 and Table 2, along with an illustration of the overlap & add scheme for determining the digital output from the comparator outputs.

$b_1(k)$	$b_2(k)$	$V_{DAC}(k+1)$	$V_o(k+1)$
0	0	$-V_{REF}$	$2V_o(k) + V_{REF}$
0	1	0	$2V_o(k)$
1	1	V_{REF}	$2V_o(k) - V_{REF}$

Table 2 Residue computation in 1.5-bit/stage scheme

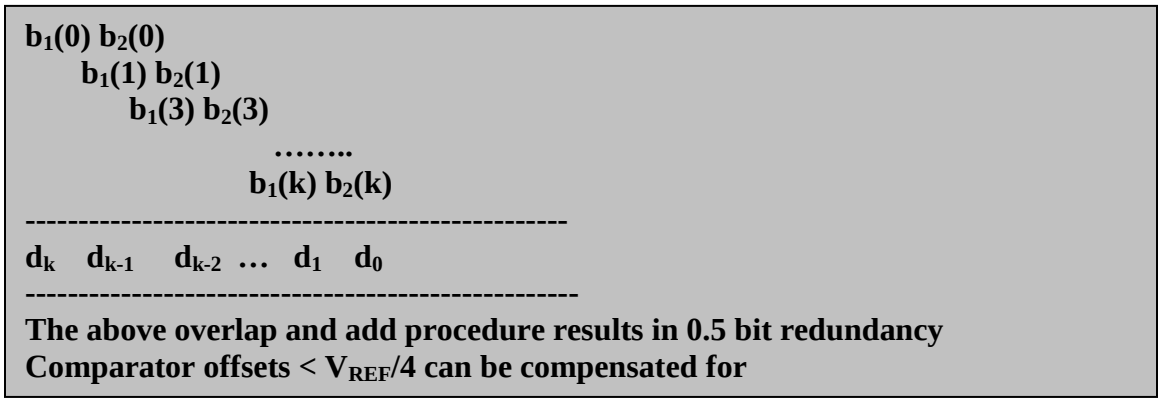

Fig. 11 Overlap & Add technique for 1.5-bit/stage scheme

System & Circuit Design

Our primary goal is to reduce the power consumption of the system to the minimum while maintaining optimal performance. This is done by turning off the entire system between successive input samples, and by placing the ADC in standby mode upon completion of each conversion cycle.

It is also desirable to use opamps with low power consumption. This has been done through the use of opamps operating in the subthreshold region. The resulting element has a remarkably low DC power consumption of 5uW. However, there are concerns regarding the reliability of the subthreshold models for the transistors used. Hence, as an alternative, we also have an opamp working in the saturation mode of operation. This consumes relatively higher amounts of power. However, it is also capable of operating at frequencies much higher than required for our application. This can be exploited by performing conversions at an accelerated pace and then placing the system in standby until the next conversion cycle, thus saving considerable amount of DC power.

This ADC was designed in a 3.3V 0.35u standard CMOS process.

Nonideal effects in algorithmic ADCs and measures for compensation

There are several nonidealities inherent in every circuit, and most of these result from the elements used including opamps, comparators and passive elements, while some are more fundamental and cannot be corrected for. Briefly summarized, these include opamp offset, finite gain and bandwidth, comparator offset and finite gain, systematic and random errors in values of passive components and reference voltages, parasitic elements, noise, nonlinearity, charge injection, clock feedthrough, clock jitter and finite slew rate of opamps. All of these manifest themselves in form of static and dynamic errors, and the design parameters need to be chosen in order to contain these errors within acceptable limits. Some of the nonideal effects may introduce errors which are relatively less malignant and hence acceptable, while some like nonlinear distortion may be utterly unacceptable. In the overall analysis, the errors are broadly classified as static and dynamic, and linear and nonlinear errors. These are described below.

Classification of errors

Linear vs nonlinear errors

An ideal ADC characteristic is shown in Fig.12. One can see that even an ideal ADC has a finite quantization error owing to resolution of the analog signal into a finite number of bits. The transfer characteristic shown below is referred to as a static or DC transfer curve. This can be affected by several different kinds of errors. There are errors like gain error or offset, the effect of which is shown in Fig. 13. These errors may or may not be acceptable depending on the application. However, in general these are considered relatively benign in most cases as they do not introduce any nonlinear distortion. However, there are errors like random mismatch which translate into nonlinear error. The nonlinear errors can be quantified in form of integral (INL), and differential (DNL) non-linear errors. An example of an ADC characteristic with nonlinear error is shown in Fig. 14. For more details, please refer [3],[4].

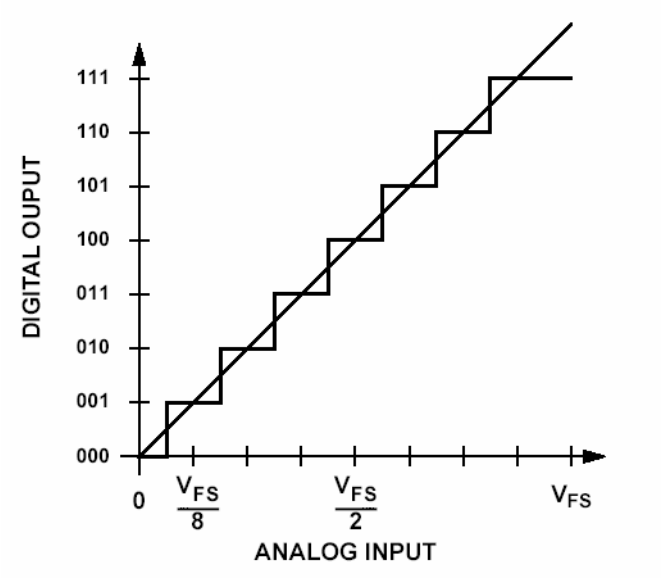

Fig. 12 An ideal ADC transfer characteristic

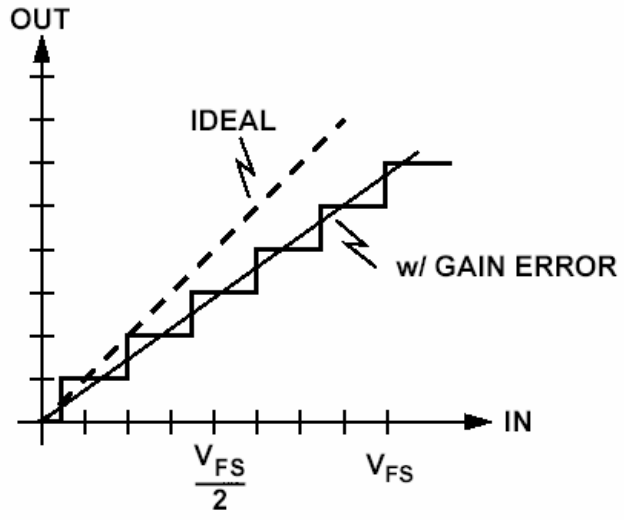

Fig. 13a ADC transfer curve with gain error

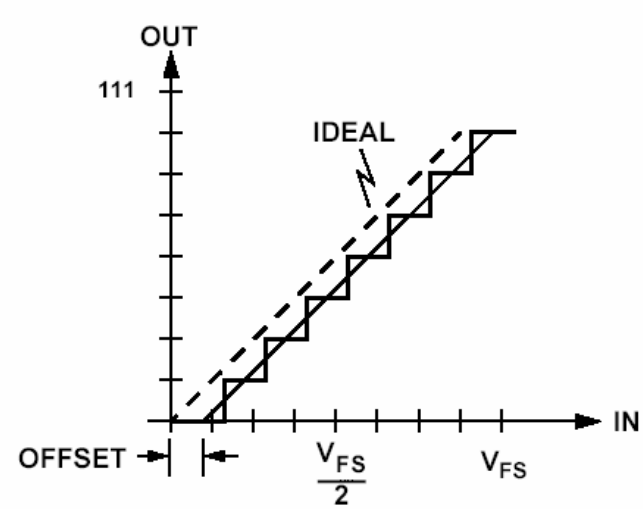

Fig. 13b ADC transfer curve with offset error

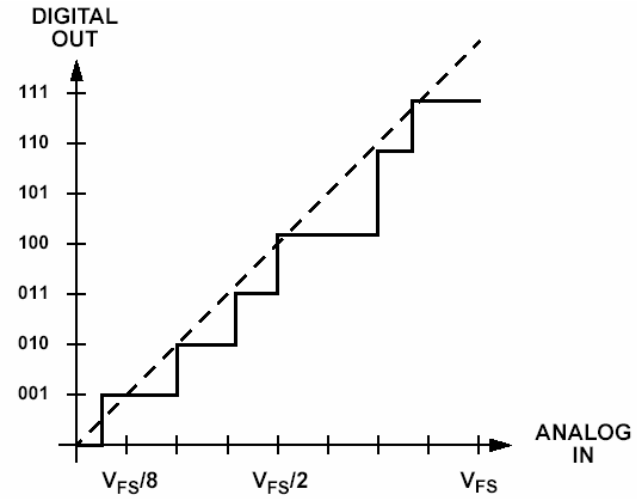

Fig. 14 ADC transfer curve with nonlinear error

In our ADC implementation, the effect of opamp offset is merely to shift the entire transfer curve up by the same amount. This is not too big a problem as it merely causes loss of a few (5-10) transition levels. The problem can be remedied by use of offset cancellation techniques but the additional cost is not justified by the small gains thus obtained. Gain error is dependent on capacitor ratio which is usually very precise (can be made accurate within 0.1%).

Static vs dynamic errors

The examples shown above were all static transfer characteristics. These represent the case where the ADC is allowed ample time to resolve the input signal, and where the various switching elements behave ideally introducing no errors of their own. However, in reality, these elements all have various limitations which translate into errors. These factors include charge-injection, clock feedthrough, finite slew rate, comparator metastability, clock jitter etc. Further details are available in [2],[3],[4]. Clock jitter is usually not too important for low-frequency operation, while the effect of the rest can be ameliorated through proper design practices.

Charge-injection is particularly virulent if it introduces signal-dependent error, and this can be remedied by the use of advanced clocks that allow us to have only charge-independent error which can be treated like a DC offset. The same applies for clock feedthrough.

Finite slew rate of the opamp is an important issue, and the opamp design must take this into account, while comparator metastability can never be eliminated in principle but the only solution lies in designing for a reasonably high gain, as the probability of a metastable occurrence is reduced exponentially with the gain.

One special problem seen especially in the algorithmic ADCs is “memory effect”. This has its origins in the finite gain of the opamp. Essentially, the effect arises owing to the fact that the parasitic capacitance at the opamp virtual ground is charged to a signal-dependent voltage. This introduces a certain degree of undesired correlation between

successive residue values and can be controlled only by appropriate choice of opamp DC gain. However, in our architecture, this effect introduces less error than the rival scheme .

One of the most important challenges involves matching the capacitors accurately. This is essential because the non-linear error introduced due to mismatch cannot be made reduced beyond the matching accuracy of the capacitors (unless sophisticated calibration techniques are used). This requires careful layout design.

Noise

Electrical noise arises owing to fundamental processes, and can be limited to a certain extent through proper design, but can never be eliminated entirely. The noise processes of interest to us are thermal noise and flicker noise. Thermal noise can result from capacitor switching (kT/C noise) or be generated within the opamp. The flicker noise originates in active devices. Flicker noise is ignored for most of the analysis as it can be compensated by the detection setup.

The important thing to note in a comparison of the proposed ADC architecture and the Nagaraj architecture is the reduction in kT/C noise in the proposed scheme. This allows us to use smaller capacitors, which in turn reduces the overall power consumption of the circuit. Thermal noise of the opamp is typically reduced by using input transistors with larger transconductance (large W/L and overdrive).

Measurements

Currently, measurement results are awaited for the proposed algorithmic ADC. The functionality has been verified through rigorous theoretical analysis and simulations. However, final estimates for linearity and power consumption can only be quoted following measurements on silicon. The current implementation is primarily intended to test the feasibility of employing the proposed architecture for low-power application. As such, it does not contain the digital circuitry required for system operation. However, this is expected to be relatively simple, and can be taken care of through the use of simple data capture and post-processing techniques. Our goal here is to assess the new architecture for performance, especially the use of subthreshold design techniques. Once

these are verified as practical, they can be used comprehensively to build a complete system operating at low-power levels.

Future directions

Apart from evaluating the proposed architecture for suitability, we have been looking for more new schemes that might offer even greater advantages in terms of performance. Our search has yielded another new algorithmic architecture offering promise of significantly greater accuracy with potential for lower power consumption. This new idea exploits ternary logic instead of binary logic and is expected to offer greater information derived for each unit of energy consumed by the conversion process. The basics of ternary conversion are described in the following sections along with the reasons for pursuing this course of action.

Ternary Converter Basics

Ternary conversion is quite similar to binary conversion except for the use of a 3-level logic. It is important to note the fact that ternary logic is fundamentally different from the 1.5-bit scenario, despite the apparent similarity in the style of implementation and use of 2 thresholds. A possible ternary SAR system is depicted below along with the relevant equations and relations (Fig 15). The SAR (Successive approximation) ADC is similar to the algorithmic ADC in terms of the underlying principle, and is merely different in implementation. While the SAR relies on a divided reference approach, the algorithmic converter works on a multiplied remainder principle. These algorithms can be modified to some extent if there is pre-knowledge of the signal content [8].

Again, our focus is on algorithmic converters as they are better suited for our task than the other options, for the reasons discussed in the section on binary Nyquist-rate ADCs. To summarize briefly, these include a simple implementation, fewer devices and reference levels, lower power consumption and moderate accuracy and speed.

There are 2 conventions used in ternary arithmetic – the signed (-1,0,1) and unsigned (0,1,2) ternary system. Although they are similar in essence, one can choose one or the other for the sake of convenience. We employ the unsigned format for our discussion and call each of the symbols "trits" (ternary digits) in analogy with "bits" (binary digits).

Why use ternary arithmetic ?

To begin with, ternary representation provides us with more information per symbol. Thus, for each step of the conversion, we obtain more information about the signal, and hence the overall conversion takes fewer steps, yielding greater amount of information per step, which translates to greater amount of information per unit energy consumed in the conversion.

If we consider the operation of a ternary SAR/algorithmic system, where the input signal V_{in} is compared to two adjustable thresholds V_{hi} and V_{lo} with $V_{hi} > V_{lo}$, then the k^{th} "trit" can be found as shown below:

$T_k = 0, V_{in} < V_{lo}(k)$

$T_k = 1, V_{lo}(k) <= V_{in} < V_{hi}(k)$

$T_k = 2, V_{in} > V_{hi}(k)$

Now, just like a number digitized into binary form, a ternary representation is also merely a quantized approximation of the analog signal, and hence exhibits quantization error. The magnitude of this quantization error goes down steadily as the number of digits used to represent the analog value goes up. Hence, the equivalent analog value of a binary and ternary number can be represented as shown below.

Binary : $V_{quantized} = B_0.2^0 + B_1.2^{-1} + B_2.2^{-2} + \ldots. + B_{(N-1)}.2^{-(N-1)}$

Ternary: $V_{quantized} = T_0.3^0 + T_1.3^{-1} + T_2.3^{-2} + \ldots. + T_{(N-1)}.3^{-(N-1)}$

Thus, the resolution of a converter is dependent on the number of digits used for representing the analog signal and the base number system. This quantization error δ can be expressed as $(1/2^N)$ and $(1/3^N)$ for N-digit binary and ternary representations

respectively. It is customary to define a signal-noise ratio (SNR) for purposes of comparison. This SNR is defined as shown below.

$$SNR = 20 \log \delta \text{ dB}$$

A comparison of SNRs for the two number systems is shown in Table 3.

Number of digits	Binary	Ternary
1	6	10
2	12	19
3	18	29
4	24	38
5	30	48
….		

Table 3 SNR trends with increasing resolution

One can see that the SNR is much greater for an N-bit ternary representation as compared to an N-bit binary representation. Thus, use of a ternary number system is beneficial in providing greater resolution for an ADC. This brings us to the next question.

Why not use higher multi-bit representations ?

One might be tempted to use higher-order quantization schemes and go beyond the 3-level system. This should provide higher resolution per step of conversion. Then, what makes the ternary system any different from any other multi-bit scheme?

The answer lies in the uniqueness of the ternary number system and its special properties. Although it might seem to be just an extension of the binary number system, in reality it is quite a different system. The underlying modulo 3 arithmetic arithmetic has properties not shared by the modulo 2 arithmetic including special redundancy features different from the ones possessed by the 1.5-bit/stage scheme, and these bestow some special advantages including the possibility of using special error correction schemes that can

help enhance the advantage offered by the ternary scheme. Currently, we are exploring this topic in order to design suitable error correction schemes.

Although the ternary scheme may superficially resemble the 1.5-bit scheme in terms of sharing 2 thresholds, one can see that even then, the residue characteristic for the ternary scheme is different (Fig.17), and so is the operation of a ternary algorithmic ADC. Moreover, a glance at the overlap & add scheme for 1.5-bit (Fig.11) shows that (N+1) binary digits are combined to yield N binary digits. However, in a ternary ADC, the N ternary outputs can be translated to 1.5 N binary digits. Hence, the information content obtained is quite high with the circuit complexity being more or less the same.

Ternary SAR conversion : Proposed approach

A possible ternary SAR converter scheme is shown in Fig.15. The DAC is the critical part of this system.

In general, the conventional approach to designing the DAC involves use of a resistor string to generate all possible reference thresholds, or use of mutiple current sources that are switched to generate these thresholds. Examples of resistor-string and switched-current based DACs are available in [3],[4]. These utilise a large number of passive or active elements and lead to a design with large area and power consumption among other issues.

Our goal in proposing a new architecture was to eliminate the need for multiple reference generation through such means, and to retain the inherent simplicity of the algorithmic structure. The system behavioral equations and the system block diagram are depicted in the Figs 16-18. This system requires 2 opamps for generation of the 2 thresholds, and the configuration is implemented in fully differential form in order to make the design more robust. Although the signal of our interest is single-ended in nature, and was the reason for a previous single-ended implementation of the binary algorithmic ADC, we have decided to choose a fully differential implementation for this new approach owing to the vast advantages conferred by such a scheme in terms of linearity, noise performance and reduction of spurious effects like charge-injection and clock feedthrough. Although the

power consumption of a fully differential circuit is nearly twice that of a single-ended system, the improvements in performance are much greater, and allow one to scale down the overall power consumption while meeting performance measures achieved by single-ended schemes at greater expense. An additional requirement would be to convert the single-ended signal to a differential form following amplification by the LNA. In addition, this system is insensitive to stray capacitances and hence quite robust.

This system has been verified for functionality by theoretical analysis and behavioral simulations using MATLAB. Sample results for a few cycles of the behavioral simulation are shown in Fig.19.

Design of the ternary system

Basic circuit design

We are currently investigating the possibility of using active elements operating in subthreshold region. The feasibility of this approach can be assessed once measurements are conducted on the first chip. This should also provide insight into possible issues, which we would need to take into account before deciding on the design parameters.

Additional features – entropy-based coding

Without loss of generality, let us consider a binary-coded system. It is well-known that direct binary coding is not the most efficient way to maximise information content, more so when the assumptions of uniformity in data are not valid. An efficient and "greedy" coding scheme is Huffman coding [7], which is widely used in various applications. This coding scheme groups together different data patterns of the basis of the probability of occurrence and assigns short symbol sequences to signal values that have a higher probability of occurrence and longer patterns to those that are less likely, thus maximizing information content per symbol.

This principle can be applied to data conversion as well, and instances of its application to SAR ADCs are available in literature [8]. It seems quite convenient to implement these in SAR as this requires only a slight modification to the existing SAR logic. Typically,

this modification is carried out by an end-user based on particular information available about the data source. However, what is not very well-known is the possibility of using the same technique to maximize information content (entropy) per unit energy in algorithmic conversion. Since algorithmic ADCs operate on exactly the same principle as SAR ADCs and differ only in terms of their implementation, it is possible to extend entropy-based coding techniques to algorithmic converters as well with slight modifications.

While in SAR ADCs the entropy-based coding is implemented by generating more probable references first through the SAR logic, this is not possible in algorithmic converters. However, what can be done is to terminate the conversion once a pattern is detected. Usually, Huffman coding is implemented in such a manner as to allow discrimination of different patterns quite easily. This can be used to prematurely end the conversion process and save energy. Similarly, the conversion process can be stopped prematurely if the resolution requirements are relaxed. All these advantages make the algorithmic and SAR ADCs quite competitive in terms of their power budget. However, for our current application, we do not have information regarding the probability distribution for the input data, and this is assumed to be more or less uniform. The use of entropy-coding techniques is thus not advisable. However, in the future, this technique can be exploited if such an approach is deemed advantageous.

Conclusions

In the past year of research, two new ADC architectures were proposed, both with potential for low-power operation. One of these was implemented on silicon with use of low-power design techniques, and test results are awaited. Current work is focused on design of a new ADC based on the second architecture.

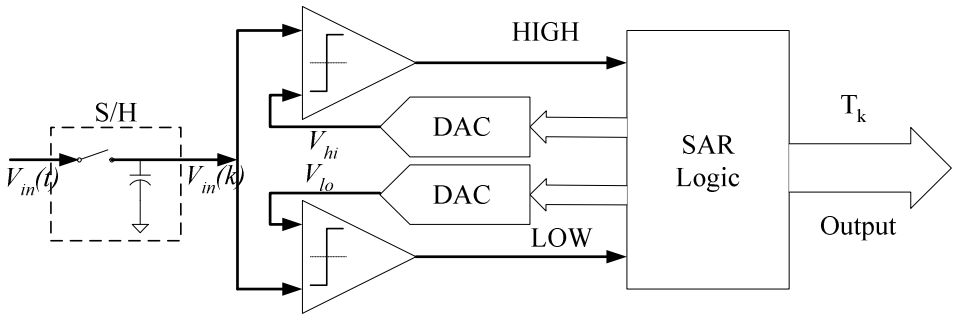

Fig. 15 A ternary SAR system

$$V_{hi}(k)=V_{B_{hi}}(k)+\Delta V_{hi}(k);V_{B_{hi}}(0)=0 \qquad V_{lo}(k)=V_{B_{lo}}(k)+\Delta V_{lo}(k);V_{B_{lo}}(0)=0$$

$$\Delta V_{hi}(k+1)=\frac{\Delta V_{hi}(k)}{3};\Delta V_{hi}(0)=\frac{2}{3} \qquad \Delta V_{lo}(k+1)=\frac{\Delta V_{lo}(k)}{3};\Delta V_{lo}(0)=\frac{1}{3}$$

$$V_{B_{hi}}(k+1)=V_{B_{hi}}(k)+\frac{(2-T_k)}{2}\Delta V_{hi}(k) \qquad V_{B_{lo}}(k+1)=V_{B_{lo}}(k)+\frac{(T_k-1)}{1}\Delta V_{lo}(k)$$

Fig. 16 Ternary algorithmic ADC operational equations for DAC

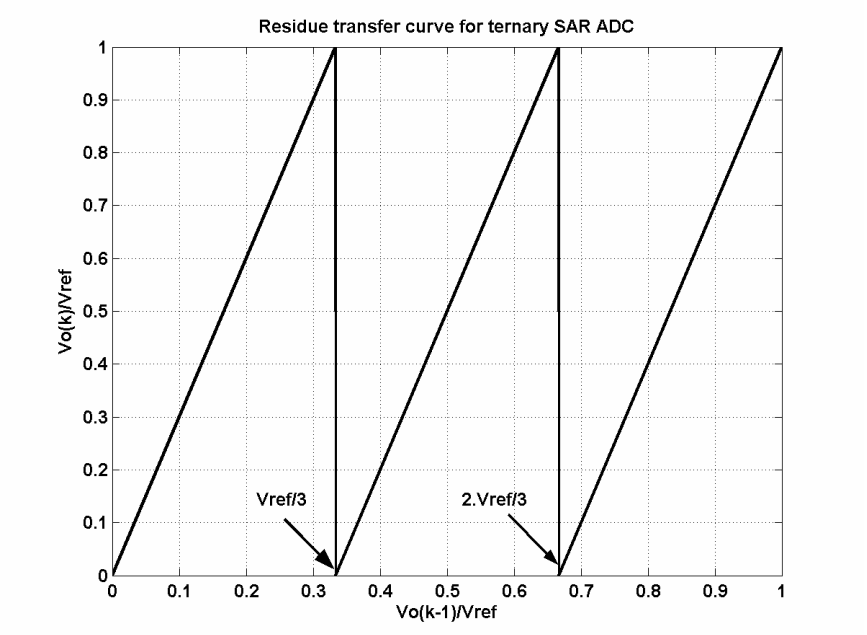

Fig. 17 Residue transfer curve for ternary algorithmic ADC

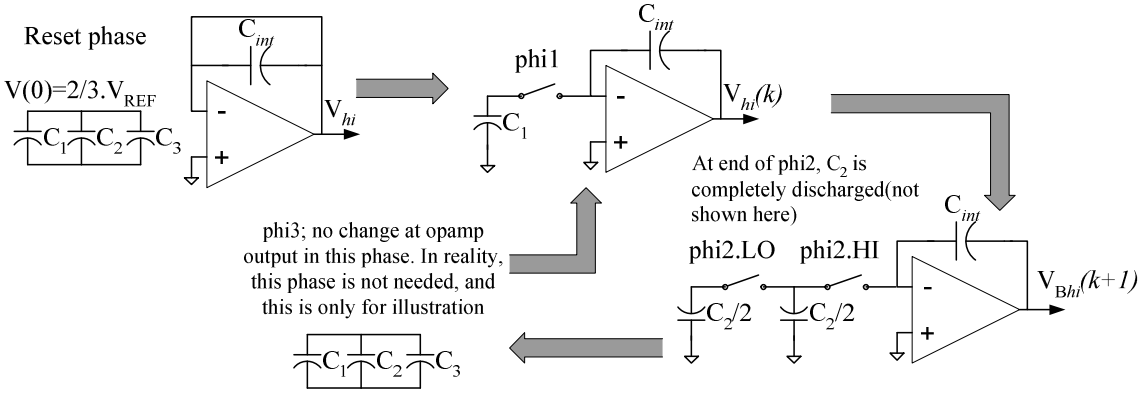

Fig. 18a Ternary algorithmic DAC for ADC (V_{hi}), shown simplified and single-ended

Output passed on to comparator only in phi1 for both cases. phi3 is symbolic and can be eliminated with use of 1 extra capacitor. The 2 circuits are independent, and capacitors for the 2 are physically separate.

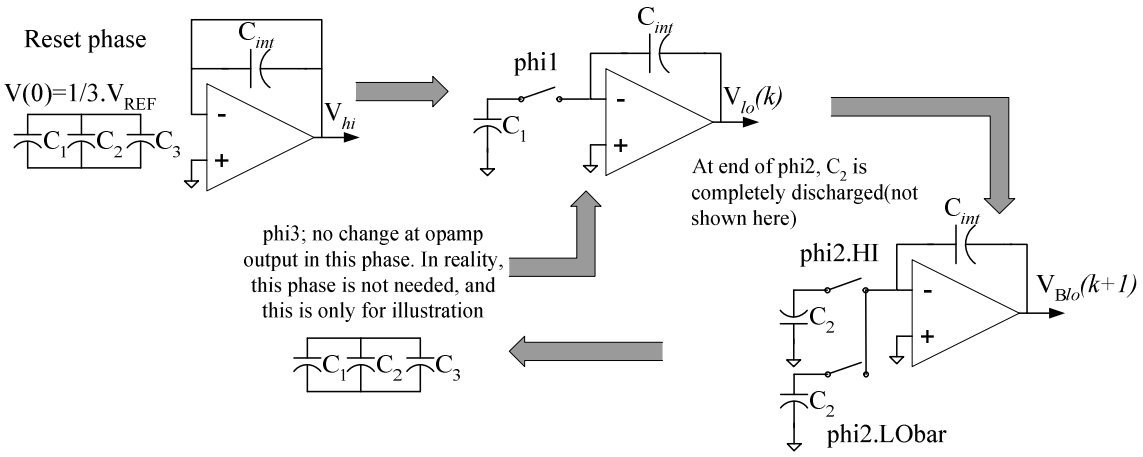

Fig. 18b Ternary algorithmic DAC for ADC(V_{lo}), shown simplified and single-ended

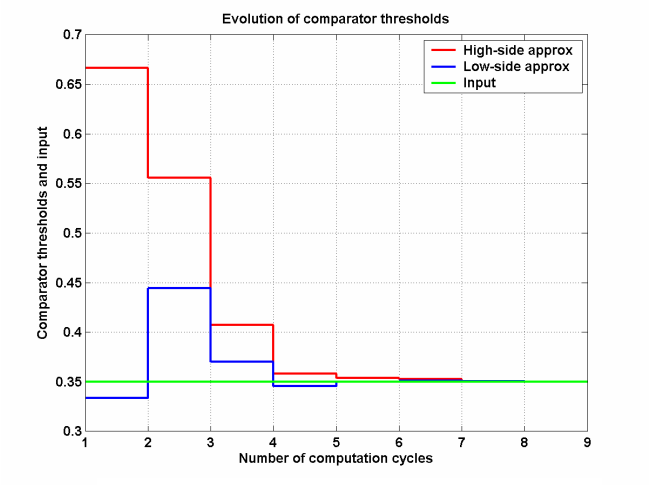

Fig. 19a Convergence of ternary ADC

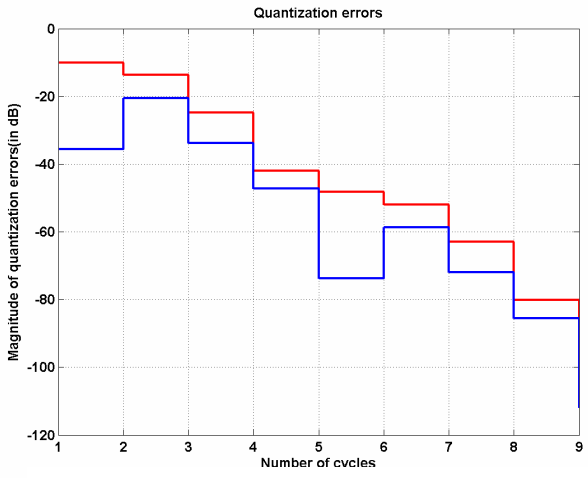

Fig. 19b SNR reduction with convergence

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